

Hao Zheng

Contact Information

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Education

M.S. and Ph.D. in Electrical Engineering 1996 – 2001
University of Utah, Salt Lake City, UT

B.S. in Electrical Engineering 1989 – 1993
Northwestern Polytechnic University, Xi'an, China

Professional Experience

Assistant Professor, the Department of Computer Science and Engineering 2004– present
University of South Florida, Tampa, FL

Research Scientist, ASIC Design Group 2001 – 2004
IBM Microelectronics Division, Burlington, VT

Research Assistant, the Department of Electrical and Computer Engineering 1996 – 2001
University of Utah, Salt Lake City, UT

Electronics Engineer, Air China 1993 – 1996
Beijing, China

Research Interests

- Formal methods in computer system design
- Parallel/distributed computing
- Reconfigurable computing systems,
- Machine learning in design automation.

Awards and Honors

- USF Outstanding Research Achievement Award, 2007.
- NSF Faculty Early Career Development (CAREER) Award, 2006.

Research Funding

- H. Zheng, “CAREER: Methodologies and Tools for Large Scale Real-Time Concurrent System Verification”, **National Science Foundation** CCF-0546492, 3/06 – 2/2011, \$400,000.
- S. Bhanja (PI), V. Jain (co-PI), N. Ranganathan (co-PI), S. Katkooori (co-PI), H. Zheng (co-PI), “CRI: Infrastructure acquisition for sub-100 nano VLSI research”, **National Science Foundation** CNS-0551621, 3/2006 – 2/2007, \$215,023,

Publications

Refereed Journal Articles

- H. Zheng, “F0: A Model Checker with Effective Compositional Methodologies for Large Asynchronous System Verification”, to be submitted to Formal Methods in System Designs.
- H. Zheng, H. Yao, T. Yoneda, “Modular Model Checking of Large Asynchronous Designs with Efficient Abstraction Refinement”, submitted to IEEE Transactions on Computers.
- H. Yao, H. Zheng, “Automated Interface Refinement for Compositional Verification”, in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 28(3), 433-446, 2009.
- H. Zheng, J. Ahrens, T. Xia, “A Compositional Method with Failure-Preserving Abstractions for Asynchronous Design Verification”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 27(7), 2008.
- T. Xia, H. Zheng, “Timing Jitter Characterization for Mixed-Signal Production Test Using the Interpolation Algorithm”, IEEE Transactions on Industrial Electronics, 54(2), 2007.
- H. Zheng, C. Myers, D. Walter, S. Little, and T. Yoneda, “Verification of Timed Circuits with Failure Directed Abstractions”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 25(3), 2006.
- H. Zheng, E. Mercer, C. Myers, “Modular Verification of Timed Systems Using Automatic Abstraction”, *IEEE Transactions on CAD*, September, 2003.

Conference Papers

- D. Mu, T. Xia, H. Zheng, “Data Dependent Jitter Characterization Based on Fourier Analysis”, Proceedings of IEEE International Symposium of Defect and Fault Tolerance in VLSI Systems (DFT), November 2006.
- T. Xia, H. Zheng, and A. Ginawi, “Self-Refereed On-Chip Jitter Measurement Circuit Using Vernier Oscillators”, IEEE Computer Society Annual Symposium on VLSI, May 2005.
- T. Xia, P. Song, H. Zheng, “Characterizing the VCO jitters due to the Digital Simultaneous Switching Noise”, ACM Great Lakes Symposium on VLSI, April 2005.
- H. Zheng, C. Myers, T. Yoneda, “Verification of Timed Circuits with Failure Directed Abstractions”, IEEE International Conference on Computer Design (ICCD’03), San Jose, CA, October 2003.
- E. Mercer, C. Myers, T. Yoneda, H. Zheng, “Modular Synthesis of Timed Circuits using Partial Order Reduction on LPN”, The Workshop on Theory and Practice of Timed Systems, April 2002.
- H. Zheng, E. Mercer, C. Myers, “Automatic Abstraction for Hierarchical Verification of Timed Systems”, International Conference on Computer Aided Verification (CAV’01), pages 182 – 193, July 2001.
- C. Myers, W. Belluomini, K. Killpack, E. Mercer, E. Peskin, H. Zheng, “Timed Circuits: A New Paradigm for High-Speed Design”, Asia and South Pacific Design Automation Conference, February 2001 (invited paper)
- H. Zheng, C. Myers, “Automatic Abstraction for Synthesis and Verification of Deterministic Timed Systems”, ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, December 2000.
- B. Bachman, H. Zheng, C. Myers, “Architectural Synthesis of Timed Asynchronous Systems”, IEEE International Conference on Computer Design (ICCD’99), October 1999.
- C. Myers, H. Zheng, “An Asynchronous Implementation of the MAXLIST Algorithm”, International Conference on Acoustics, Speech, and Signal Processing, April 1997.

Ph.D. Dissertation

- Modular Synthesis and Verification of Timed Circuits Using Automatic Abstraction, University of Utah, 2001.

Teaching

University of South Florida (2004 - present)

- CIS 4930, Design Automation, Spring 2009
- CDA 4253, FPGA System Design, Fall 2006, 2008.
- CDA 5416/CIS 4930, Introduction to Computer-Aided Verification, Spring 2008
- COT 3100, Introduction to Discrete Structures, Fall 2007.
- CIS 4930/CIS 6930, Introduction to Computer-Aided Verification, Spring 2006, 2007.
- CIS 4930, FPGA Design, Fall 2004, 2005.
- CIS 6930, Asynchronous Circuit Design, Spring 2005

Students Advised

Current Students:

- Haiqiong Yao (Ph.D.) 2006 - present
- Nicholas Donataccio (Ph.D.) 2008 - present

Former Graduate Students:

- Ryan Mabry (M.S., co-advised with Dr. Nagarajan Ranganathan) 2007
Recipient of 2007 USF Outstanding Thesis Award
- Jared Ahrens (M.S.) 2007

Undergraduate Research Students

- Christopher Earl, REU student 2007
- Halam Le, REU student 2007
- Paul Ireif, REU student 2006
- Ryan Marby, Honors Thesis 2005

Invited Talks

- NEC Labs America, Princeton, NJ, 2/2009.
- IBM Austin Research Lab, Austin, TX, 2/2009.
- University of Florida, Gainesville, FL, 11/2008.
- Portland State University, Portland, OR, 11/2008.
- University of Utah, Salt Lake City, UT, 8/2007.
- Xidian University, Xi'an, PRC, 5/2006.

Services

IEEE member

- Technical program committee, HLDVT 2009, IEEE International High Level Design Validation and Test Workshop.
- Technical program committee, ISVLSI 2009, IEEE Computer Society Annual Symposium on VLSI.

Reviewer for:

- National Science Foundation, panelist, 2006.
- A proposal from Netherlands Organization for Scientific Research, division Physical Sciences
- **Journals:**
 - Formal Methods in System Design
 - IEEE Transactions on Computers
 - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
 - IEEE Transactions on Very Large Scale Integration Systems
 - ACM Transactions on Design Automation of Electronic Systems
 - IEE Proceedings of Computers and Digital Techniques
 - Transitions on Information Processing Society of Japan
 - Louisiana Board of Regents RCS proposal
- **Conferences:**
 - 2008 : DATE09
 - 2006 : ISCAS and DAC.
 - 2005 : DAC and GLVLSI.

Services to the University

- Reviewer for USF College of Engineering CAREER reviewing panel Summer 2008
- Faculty advisor of the IEEE Computer Society USF Chapter 2006– present
Won **Best Student Organization of College of Engineering** award (2009) .
- Member of the Undergraduate Committee, CSE Dept., USF 2004– present