Design Methodologies for High Density Domain Wall Memory
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Abstract — Domain wall memory (DWM) has emerged as a possible candidate for embedded cache application. The fundamental advantage of DWM is its MLC (multi-level cell) capability allowing it to store multiple bits/cell in order to break the density barrier. Additionally, it provides low standby power, fast access time, good endurance and good retention. In this paper, we address design challenges associated with DWM for potential use in on-chip cache.

Keywords— High density memory, Domain wall memory.

I. INTRODUCTION AND MOTIVATION

The unprecedented demand for bandwidth (BW) in future power constrained high end graphics processors would require fundamental changes in the way we design cache. There is already a ~2X BW gap between CPU and external memory today which will worsen if appropriate measures are not taken to fill the BW gap [1]. Semiconductor industry has started embracing emerging high density embedded memories such as eDRAM and STT-RAM that are 4-10X dense compared to SRAM in order to meet the near term BW requirement [2]. However, future bandwidth intensive applications would need 20-50X denser memories with extremely low standby power. Monolithic stacking using 3D technology is one possible solution to virtually increase the density however that would be obstructed by extra mask cost, yield and thermal challenges. Die-to-die stacking would require expensive through-silicon-vias. Hence, it is necessary to develop circuit and system design methodologies for embedded memories that are scalable, low power and possesses high MLC capability.

Domain wall memory (DWM) [3] has been explored as a possible candidate for data storage. The fundamental advantage of these memories is its MLC capability allowing it to store multiple bits/cell in order to break the density barrier. Additionally, it provides low standby power (due to its non-volatility), fast access time, good endurance and good retention [2]. DWM based array has been proposed for cache application in [4] and a 256 bit in-plane DWM array has been experimentally demonstrated by IBM [5]. However, the subarray architecture and peripheral circuit designs have not been addressed. DWM memories have great potential to be used as on-chip random access cache however very little effort has been spent to-date to address numerous circuit and system design challenges associated with these memories. In this paper, we make following contributions:

- We address subarray organization issues like bitcell arrangement, addressing structure, bitcell layout, number of DW per NW etc.
- We develop methodology for DWM subarray design. This includes bitcell and peripheral circuits with their sizing strategy.

The paper is organized as follows. A brief overview of DWM is provided in section II. The subarray architecture is presented in Section III. The sizing approach and detailed circuit challenges and solution are discussed in Section IV. Finally, conclusions are drawn in Section V.

II. DOMAIN WALL MEMORY

There are three important components of DWM- write head, read head and magnetic nanowire (NW) as shown in Fig. 1. The read/write heads are essentially similar to conventional MTJ whereas NW is analogous to shift register. New bits are written into NW through write MTJ. shift is performed by injecting of charge current (through LS and RS) to shift the bits in lockstep fashion and read is performed by bringing the desired bit under the read head and sensing the resistance of the read MTJ. Magnetic NW stores the bits in terms of magnetic polarity that could be in-plane or perpendicular to the plane. Perpendicular magnetic anisotropy (PMA) materials provide improved thermal stability so it is ideally suitable for use as read head. Lower domain wall nucleation
In this section, first we present the simulation setup. This is followed by amplifier (#14). Current of high and low resistance by using current mirroring in load small voltage on the rBL. A reference circuit (#17) provides average the desired domain under the read head and sensing it by providing a followed by a shift operation to bring the new domain under the write column in parallel is illustrated in Fig. 4(g). In order to supply a constant current, the PMOS needs to stay in saturation. However, our simulation shows (Fig. 4(h)) that the voltage drop across DW pushes the PMOS to line and subsequently to cut-off when number of bits in the NW increases beyond 12. The size of shift transistor needs to be increased to sustain minimum shift current at the cost of area overhead. (b) Number of NW per shift circuitry: Our simulation reveals that one shift circuit can handle shifting of 48 columns in parallel. This is due to shift interconnect resistance that prevents last column from getting minimum shift current. Designing subarray with more than 48 rows would require extra shift circuitries. (c) Variation in DW resistance: Fig. 4(i) indicates the impact of resistance variation on shift current. It is evident that 15% change in DW resistance (nominal value is 200 ohms) can induce ~12% change in shift current. This essentially means that the shift circuitry needs to be robust enough to absorb this variation.

4.5 Subarray specifications and other challenges: The number of rows and columns in the subarray depends on the factors like WL speed after periodic strapping, optimal BL length to meet read access time, shift speed etc and needs careful evaluation. Position of read and write head is another challenge that needs careful considerations.

V. CONCLUSIONS

We provided design methodologies for DWM array and discussed several circuit trade-offs. Our study indicates that successful demonstration of DWM as last level cache would require detailed modeling and simulation of MTJ and DW with carefully crafted peripheral circuitries.

REFERENCES