

Ransford Morel Hyman Jr.
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Objective	To obtain a job position as an Design/Reliability/CAD Engineer.	
Education	Ph.D. in Computer Science and Engineering <i>University of South Florida, Tampa, FL.</i> <i>Concentration: Fault Tolerance and Reliability in CMOS VLSI Designs</i> G.P.A. 3.48/4.0	2011 2010
	M.S. in Computer Engineering <i>University of South Florida, Tampa, FL.</i> G.P.A. 3.5/4.0	2006
	B.S. in Mathematics <i>Bethune-Cookman University, Daytona Beach, FL</i> Concentration in Algebra and Number Theory G.P.A. 3.5/4.0	
Relevant Coursework	Computer Architecture • CMOS VLSI • VLSI Algorithms and Architecture • Digital Circuit Synthesis • Integrated Circuit Technology • Compiler Design Techniques • Operating Systems • Algorithms • Advanced Algorithms	
Experience	Instructor, Florida Education Fund <ul style="list-style-type: none">• Worked with high school students to enhance their problem solving skills and awareness of various SAT Math problems.• Facilitated Career Planning course focused on how to choose and obtain their ideal career goals.	2009
Skills	<ul style="list-style-type: none">• Programming skills: C/C++, Perl, Verilog, VHDL, Tcl, Bourne C-Shell Shell Scripting.• Synopsys EDA Tools: Design Compiler, Verilog Compiler Simulator(VCS), Primetime-PX.• Cadence EDA Tools: Virtuoso Custom IC suite, RTL Compiler, SoC Encounter• Operating Systems: Microsoft Windows 95/98/XP/Vista, Sun Microsystems Solaris 8 or better, Linux• Research tools: SPLASH/SPLASH2 and ISCAS '85 benchmarks, OpenCores Circuits, and RSim Micro-architecture Simulator.	

Memberships & Awards

Member, Institute of Electrical and Electronics Engineers(IEEE) – Computer Society
Member, National Society of Black Engineers
President, IEEE – Computer Society University of South Florida Student Chapter

- Awarded Best Student Organization at University of South Florida Engineering Expo.

Recipient, NSF-FGLSAMP Bridge to Doctorate Fellowship
Recipient, Florida Education Fund Mcknight Doctoral Fellowship.
Recipient, 2009 Florida Education Fund Crawford Award for my outstanding performance as Instructor for the Florida Education Fund.

Publications

- Hyman,R; Bhattacharya,K.;Ranganathan,N.;, “A strategy for soft error reduction in multi core designs,” Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on, vol., no., pp.2217-2220, 24-27 May 2009
- Hyman Jr.,R., Bhattacharya,K.;,Ranganathan,N.;, “Redundancy Mining for Soft Error Detection in Multi-core Processors,” Computers IEEE Transactions on, vol.PP,no.99,pp.1-1, 0

doi:10.1109/TC.2010.168

- Mahalingam, V. Ranganathan, N., Hyman Jr., R.; "A Variation Tolerant Circuit Design technique using Dynamic Clock Stretching," Emerging Technologies, ACM Journal of, June 2011. (Submitted and Under Review)
 - Hyman Jr., R, Bingel, T., Ranganathan, N., Vo, D.T.,; "A Clock Control Strategy for Peak Power Reduction Using Pth Clustering," Very Large Scale Integration, IEEE Transactions on, June 2011. (Submitted and Under Review)
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