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EDUCATION

Doctor of Philosophy - Computer Science, August 1988, University of Central Florida, Orlando
Dissertation: Hardware Algorithms for Data Compression

Bachelor of Engineering (Honors) - Electrical & Electronics, May 1983
Regional Engineering College, Tiruchy, University of Madras, India

EMPLOYMENT

Assistant Professor: July 1988 to July 1993; **Tenured Associate Professor:** August 1993 to July 1998; **Professor:** August 1998 to July 2007; **Distinguished University Professor** since August 2007, Dept. of Computer Science and Engineering, University of South Florida, Tampa.

Professor, Dept. of ECE, University of Texas at El Paso, from Sept 1998 to May 1999.

Graduate Research / Teaching Assistant, Dept. of Computer Science, University of Central Florida, Orlando, January 1984 to April 1988.

Systems Executive, International Computers Limited (U.K.), Bombay, India. June 1983 to Dec 1983.

RESEARCH AREAS

Primary research areas are VLSI system design, VLSI design automation, hardware algorithms, computer architecture, and biomedical information processing. Other interests include parallel processing, data compression, and VLSI for vision, video, image processing, pattern recognition and biometrics. Current projects include application of economic models and game theory to VLSI design, resource and emergency management for homeland security applications, modeling process variations for circuit optimization, power optimization at architectural and circuit levels, 3-D volumetric medical image rendering, and low power synthesis of programmable cores in SOC systems.

COURSES

Undergraduate: Computer Organization and Architecture, Introduction to CMOS VLSI Design

Graduate: Advanced Computer Architecture I, Advanced Computer Architecture II, Parallel Processing, CMOS VLSI Design, VLSI Algorithms and Architectures, and Bio-information Processing.

AFFILIATIONS

Fellow of the IEEE, (S-'81, M-'88, SM-'93, F-'02)

Member of the IEEE Computer and Circuits & Systems Societies

Member of the VLSI Society of India

HONORS AND AWARDS

- **Distinguished University Professor** title and university gold medallion honor, 2007.
- **USF Graduate Council Outstanding Thesis Award**, Major Professor to R. Mabry, Power Estimation in Asynchronous Circuits Using Petrinets, Aug 2007.
- **Best Paper Award, ranked 1 out of 360 submissions**: N. Hanchate and N. Ranganathan, "A Linear Time Algorithm for Wire Sizing with Simultaneous Optimization of Interconnect Delay and Crosstalk Noise", Proc. Intl. Conf. on VLSI Design, Jan 2006.
- **Best Paper Award, ranked 1 out of 330 submissions**, Intl. Conf. on VLSI Design, Jan 2004, "Gate Sizing and Buffer Insertion Using Economic Models for Power Optimization," co-authored with A. Murugavel.
- **Best Paper Award, ranked 1 out of 139 submissions**, Intl. Conf. on VLSI Design, 1995, "JAGUAR: A VLSI Chip for JPEG Image Compression Standard," co-authored with M. Kovac.
- **Best Paper Award Nominations, ranked within top 6-8 papers based on independent/blind reviews, forwarded to the Best Paper Award Panel**, Intl. Conf. on VLSI Design, 1995,98,00,02,04,06.
- **USF Theodore and Venette Askounes-Ashford Distinguished Scholar Award**, 2003.
- **SIGMA XI Scientific Honor Society Tampa Bay Chapter Outstanding Faculty Researcher Award**, 2004.
- **USF President's Award for Faculty Excellence**, 2002-03.
- **USF Division of Sponsored Research Outstanding Research Achievement Award**, 2002.
- **Fellow of IEEE**, *for contributions to algorithms and architectures for VLSI systems design*, Jan 2002.
- **Editor-In-Chief**, IEEE Transactions on VLSI Systems, two terms, Jan 2003 to Jan 2007.
- **USF Graduate Council Outstanding Dissertation Award - Major Professor**, for A. Murugavel, Power Estimation and Optimization in VLSI Circuits, 2003.
- **SIGMA XI Tampa Bay Chapter Outstanding Dissertation Award - Major Professor** for A. Murugavel, Power Estimation and Optimization in VLSI Circuits, 2003.
- **USF Graduate Council Outstanding Dissertation Award - Major Professor**, for R. Chandramouli, Theory and Application of Sequential Detection under Dependence, Jan 1999.
- **USF Graduate Council Outstanding Dissertation Award - Major Professor**, V. Krishna, High Level Techniques for Power Estimation, Analysis and Optimization, Jan 1999.

- **USF Graduate Council Outstanding Dissertation Award - Major Professor**, R. Sastry, VLSI Architectures for Pattern Matching and Recognition, Aug 1994.
- **SIGMA XI Tampa Bay Chapter Outstanding Dissertation Award - Major Professor**, R. Sastry, VLSI Architectures for Pattern Matching and Recognition, Aug 1994.
- **Certificate of Appreciation** (associate editor of IEEE Trans. Video Technology), IEEE Circuits & Systems Society, 2000.
- **Certificate of Appreciation** (associate editor of IEEE Trans. Circuits & Systems, TCAS-II), IEEE Circuits & Systems Society, 1999.
- **Certificate of Appreciation** (for service as associate editor of IEEE Transactions on VLSI Systems), from IEEE Circuits and Systems Society, 1997.
- **Certificate of Appreciation** (for distinguished service in student activities), from IEEE Computer Society, February 1996.
- **Outstanding Researcher Award**(\$1000), 1995, USF College of Engineering.
- **IEEE Computer Society Distinguished Visitor Program Speaker**, 1995-03.
- **Outstanding Young Investigator Award** (\$1000), 1991-1992, in recognition of research, University of South Florida College of Engineering.
- **IEEE Computer Society R. E. Merwin Fellowship Award** (\$3000), 1987-88, for academic achievement, leadership and service to IEEE Computer Society student chapter at UCF-Orlando.
- **Rotary Foundation Graduate Fellowship** (\$20K), 1984-85, awarded by the Rotary Foundation of the Rotary International, Washington D.C., District 320 - includes four states in S. India and Sri Lanka.
- **IEEE Region X Outstanding Student Branch Chairman Award** (\$500), 1982. Region X includes India, China, Japan, Australia, New Zealand and other Southeast Asian countries.
- **IEEE Outstanding Student Award**, 1981-82, from IEEE Past-President Dr. James B. Owens for contributions towards IEEE activities as a student.
- **Rotary Foundation Youth Merit Award**, 1982, as outstanding student of Rotary District 320.
- **National Merit Certificate**, 1978, from Central Ministry of Education, Govt. of India for 19th rank out of about 250,000 students in the Higher Secondary School State-wide Examinations.
- **Isaac Daniel Gold Medal**, 1977, outstanding student in Tanjore City, based on academics, sports, quiz and debate teams, 1977.
- **Marsh Gold Medal**, 1977, awarded by the Union Club of Tanjore for First rank in the Higher Secondary School State-wide Examinations.
- **Koilpillai Good Conduct Certificate and Prize**, St. Peter's High School, Tanjore, India, 1977.
- **Bible Study Gold Medal**, St. Peter's High School, 1977.

PROFESSIONAL ACTIVITIES

- Associate Editor, ACM Transactions on Design Automation of Electronic Systems, 2007-2010.
- Steering Committee Member, IEEE Transactions on VLSI Systems, 2007-08.
- Steering Committee Member, IEEE Transactions on NanoBioScience, 2007-08.
- Editor-in-Chief, IEEE Transactions on VLSI Systems, 2003-06.
- EIC Search Committee, IEEE Transactions on VLSI Systems, Dec 06.
- Best Paper Awards Panel for IEEE Circuits and Systems Society, 2002-05.
- Outstanding Young Author Award Panel for IEEE CAS Society, 2002-05.
- Steering Committee Chair, IEEE Trans. VLSI Systems, 2001-02.
- Steering Committee Member, IEEE Trans. VLSI Systems, 1999-00, 2007-08.
- IEEE Computer Society Technical Committee on VLSI (TCVLSI) Chair, 1997-2001.
- Associate Editor, IEEE Trans. on Circuits & Systems, 1997-99.
- Associate Editor, IEEE Trans. on CAS for Video Technology, 1997-00.
- Associate Editor, IEEE Trans. on VLSI Systems, 1995-1997.
- Associate Editor, Pattern Recognition Journal, 1993-02.
- Editorial Board, International Journal of VLSI Design, since 1994.
- Editor, Special Issue on VLSI, Intl. Jour. of Pattern Recognition & Artificial Intelligence, (9)2, 1995.
- **IEEE Computer Society Activities:**
 - IEEECS Distinguished Visitors Program Speaker, 1995-2001.
 - IEEE/ACM CSE Curriculum Task Force (national level), 2004-06.
 - Executive Committee Member of IEEECS SAC, 1993-95.
 - Executive Member, IEEECS Membership Activities Board MAB, 1996-97.
 - Executive Member, IEEECS Educational Activities Board EAB, 1996-97.
 - Coordinator, IEEECS intl. student newsletter *looking forward*, 1996-1998.
 - Faculty Advisor, IEEECS Student Chapter, Uni. of S. Florida, 1990-1998.
- **Conferences Organization:**
 - Program Co-Chair, Intl. Conf. on VLSI Design, Jan 2008.
 - Design Tools Track Chair, Program Committee, Intl. Symp. Quality of Electronic Design, 2007, 2008.
 - Best Paper Award Panel, ISLPED 2006.
 - Best Paper Award Panel, Intl. Conf. on VLSI Design, 2007, 2008.
 - Steering Com. Member, Intl. Conf. on VLSI Design, 1992-Present.
 - Steering Com. Member, IEEECS Annual Symposium on VLSI, 1992-present.

- Steering Com. Member, Intl. Symp. Quality of Electronic Design, 2000-02.
- General Chair, IEEECS Annual Symposium on VLSI, Tampa, Feb 2005.
- Program Committee Track Chair, Intl. Sym. on Low Power Electronics and Design, 2006.
- Program Co-Chair, IEEECS Annual Symposium on VLSI, Tampa, Feb 2003.
- Publications Chair and IEEE Liaison, Intl. Conf. on VLSI Design, 2003, 2004, 2006.
- General Chair, IEEECS Annual Workshop on VLSI, Orlando, April 1999.
- General Co-Chair, IEEECS Workshop on VLSI, Orlando, April 1998.
- General Co-Chair, Intl. Conf. on VLSI Design, Madras, Jan 4-7, 1998.
- Publicity Chair, Intl. Workshop on CAMP, Boston, Oct 20-22, 1997.
- Workshop Chair, IEEECS Workshop on VLSI, Orlando, April 1998.
- Program Chair, IEEECS Workshop on VLSI, Clearwater, Nov 3-6, 1996.
- Publicity Chair, Intl. Conf. on VLSI Design, 1992, 1996, 1997.
- General Co-Chair, Intl. Conf. on VLSI Design, New Delhi, Jan 1995.
- Panel Moderator, Intl. Conf. on Parallel Processing, 1995.
- Program Chair, Intl. Conf. on VLSI Design, Calcutta, Jan. 1994.
- IEEE Liaison, Intl. Conf. on VLSI Design, 1993, 1999-2008.
- Local Arrangements Chair, IEEECS VLSI Workshop, Tampa, Feb 2-5, 1992.
- Best Paper Award Panel, Intl. Conf. VLSI Design, 1996, 99, 2001.

• **Conferences Program Committee Member:**

- Intl. Conference on Parallel Processing, ICPP, August 15-17, 1995;
- Intl. Symposium on Parallel and Distributed Processing, SPDP, 1995.
- Intl. Conf. on High Performance Computing, ICHPC, 1995-1997.
- Intl. Parallel Processing Symposium, IPPS, Santa Barbara, April 1995.
- Intl. Conf. on Computer Design, ICCD, 1994-1997, 1999, 2002-06.
- Intl. Conference on VLSI Design, 1993-2008.
- IEEE Computer Society Annual Workshop on VLSI, 1992-1999, 2002.
- IEEECS Intl. Symposium on VLSI, 2003-07.
- IEEE Great Lakes Symposium on VLSI, GLSVLSI, 1998, 2002, 2008.
- Intl. Workshop on Asynchronous Systems, ASYNC, 1999, 2000.
- Intl. Workshop on Design, Test and Applications, WDTA99, Croatia.
- Intl. Conf. Parallel & Distr. Proc. Techniques & Applns., PDPTA99.
- Microelectronic Systems Education Conference, 1999, 2000-05.
- Intl. Sym. on Quality of Electronic Design, 2000-01.
- Intl. Sym. on Low Power Electronics and Design (ISLPED), 2004-08.
- Intl. Sym. on Circuits and Systems (ISCAS), 2006.
- Intl. Conference on Computer Aided Design (ICCAD), 2006, 2007.

- Intl. Conference on Computer Architectures for Machine Perception (CAMP), 1997, 2000, 2003, 2006.

- **Conferences Session Chair:**

- VLSI Algorithms, Intl. Conf. on VLSI Design, New Delhi, Jan 4-8, 1991.
- Layout, Fifth Intl. Conf. on VLSI Design, Bangalore, Jan 4-8, 1992.
- Special Purpose Architectures, Sixth IPPS, Beverly Hills, Mar 23-26, 1992.
- VLSI for Machine Vision, SPIE Conf. on Applications of AI X: Machine Vision and Robotics, Orlando, April 20-24, 1992.
- DSP, Intl. Conf. on VLSI Design, Bombay, Jan 4-7, 1993.
- Computer Arithmetic, Intl. Conf. on Computer Design, Boston, Oct 1994.
- Architecture/Design, Great Lakes Symposium on VLSI, Buffalo, Mar 1995.
- Special Purpose Architectures, 9th IPPS, Santa Barbara, April 1995.
- Algorithms on Networks I, ICPP, Wisconsin, Aug 1995.
- Arithmetic Modules, Intl. Conf. on Computer Design, Austin, Oct 1995.
- Image Processing, ICHPC, High Performance Computing, Dec 27-30, 1995.
- Arithmetic Circuits, ICCD, Austin, Oct. 7-9, 1996.
- VLSI, Computer Arch. for Machine Perception, Boston, Oct 20-22, 1997.
- VLSI Architectures I, Intl. Conf. on VLSI Design, 2002.
- Low Power, IEEE Symposium on Low Power Electronics and Design, 2002.
- Low Power, International Conference on VLSI Design, 2004.
- VLSI Circuit Design, GLSVLSI, 2008.

- **Review Work:**

National Science Foundation SBIR Panel, 2007.

National Science Foundation ITR Panel, 2003, 2004.

National Science Foundation Design Automation Panel, 2003, 2006.

VLSI RISC Architectures and Organization by S. Furber, book review appeared in Journal of Computer Systems Science and Engineering, 6(1), Jan 1991;

Parallel and Distributed Computing Handbook by A. Zomaya, book review appeared in IEEE Concurrency Magazine, 5(3), Sept 1997;

- **Reviewer for journals:**

IEEE Trans. on Computers, VLSI Systems, Computer Aided Design, Circuits and Systems, SMC, Parallel and Distributed Processing, CSVT, Signal Processing and PAMI, IEEE Computer, Proc. of IEEE, IEEE Micro, Machine Vision and Applications Journal, Journal of Parallel and Distributed Computing, IEEE Design and Test, Pattern Recognition Journal, Pattern Recognition Letters.

- **Reviewer for Conferences:**

IEEE Robotics and Automation, IROS, Phoenix Conf. on Computers and Comm., ICPP, ICCD, ISCAS, ICCAD, MSE, ISVLSI, ISQED, ISLPED, IPPS, SPDP, MPPS, VLSI Design, CAMP, and DAC (for many years).

- **Service at USF:**

Faculty search committee chair (2003-2005, CSE Dept hired 6 tenure track and 5 non-tenure track faculty); Faculty search committee member (2000-05,07); CSE chair search committee (2003-04); EE chair search committee (2003-04); CSE graduate program committee (1989-98,99-03); Graduate/Ph.D. Qualifiers Examination Committee (1988-98,99-07); Faculty Governance Committee for College of Engineering (1999-2005); NNRC advisory committee (2004-06); CMR executive committee (1994-98); CSE library representative (1993-1997); CSE awards committee chair (1994-95); CSE infrastructure committee chair (2006-07); CSE strategic planning committee (2004-05); USF graduate council awards committee (2003-04); CSE undergraduate curriculum committee (1999-03).

GRANT FUNDING

1. "Multi-metric Optimization Considering Process Variations in Deep Submicron and Nanometer Design", \$315K, PI, Semiconductor Research Corporation, (\$270K from SRC and \$45K from USF), 2007-2010.
2. "The Tessera Project: A New Image Registration Algorithm and Its FPGA Realization for UAV", \$48,121, Tessera, PI with Co-PI Dr. R. Murphy, 2007.
3. "CRI: Infrastructure Acquisition for Sub-100 Nano-VLSI Research", \$215,023, National Science Foundation, Co-PI with PI S. Bhanja, 2006.
4. "Dynamic Resource Allocation for Urban Multi-Event Crisis Management", \$179,179 (\$59,179 from I-4 High Tech Corridor Initiative and \$120K from Aeolus Systems), 2004.
5. "A Game Theoretic Framework for VLSI Design Automation", \$40K, Semiconductor Research Corporation (SRC), 2004.
6. "SKINS: Sensory Knowledge-Based Interface Science - IGERT", \$3,440,280, National Science Foundation, Co-PI and Project Co-Director, 2003-2008.
7. "IEEE Transactions on VLSI Systems EIC Funding" from IEEE, \$130K, 2003-06.
8. "Dynamic Task Scheduling in Heterogenous Computing Systems", \$143K (\$105K from Tandel Systems Inc. and \$38K from I-4 High Tech Corridor Initiative), 2002-03.
9. "Mapping Applications to Networked Heterogenous Computing Systems", \$102K (\$68K from Honeywell and \$34K from I-4 High Tech Corridor Initiative), 2001-02.
10. "Switching Activity Estimation Using Bayesian Networks", \$195K, National Science Foundation, 2001-2004.
11. "Task Assignment and Scheduling for Heterogenous Computing Systems", \$93,244 (\$65K from Honeywell and \$28,244 from I-4 High Tech Corridor Initiative), 2000-01.
12. "Design of System/RT Level Power Estimator Tool", \$27,000 (\$15K from Honeywell, Clearwater and \$12K from I-4 High Tech Corridor Initiative), 1999-00.
13. "Introducing Design into Undergraduate Computer Sci. and Eng. Curriculum", \$659,734 (\$286,210-USF), National Science Foundation, 1995-1999, Co-PI with P.M. Maurer, L.K. John.
14. "Hardware and Software Design for Image Reconstruction", \$98,165, jointly with Dynacs Engineering Co., NASA TRP RAMP Program, 1996-1997.

15. "VLSI Architectures for Pattern Matching and Recognition", \$196,968 (\$138,190 from NSF and \$58,778 USF matching), MIPS 9407034, 1994-1998.
16. "Hardware and Software Design for Real-Time Multimedia Applications," jointly with Dynacs Engineering Co., NASA TRP RAMP Program, \$116,604, 1995-1996.
17. "VLSI Hardware for Image Processing," Dynax Engineering Inc., \$25,755, 1996-97.
18. "Hardware/Software Design for High Performance Computing in Simulation Environments," jointly with Dynacs Engineering Co., NASA TRP RAMP Program, \$97,349, 1994-95.
19. "Parallel/VLSI Algorithms for Data Compression," \$123,438, Florida High Technology and Industry Council, 1990-1995.
20. "Software Development and Testing," \$6,875 from Dynax Engineering Inc., 1994.
21. "Computer Vision Hardware/Algorithms", \$11,020, Insight Control Systems, 1995.
22. "Graduate Student Support", \$13,236, Danka Industries Inc., 1995-96.
23. "MOSIS Fabrication of VLSI design Projects," \$32,800, NSF-DARPA Program, 1990-94.
24. "Reduced Cycle Nonlinear Multi-function Chips," \$264,927 (\$171,000 from National Science Foundation and \$93,927-USF) 1991-93, Co-PI with V. Jain, D.L. Landis, MIP-9103286.
25. "VLSI Algorithms and Architectures for Image Processing," \$100,160 (\$70,000 from National Science Foundation, 1990-1993 (\$30,160 USF matching) - MIP-9010358.
26. "VLSI Hardware for Performance Improvement in a Relational Database System," \$8000, College of Engineering, University of South Florida, 1989-91.
27. "VLSI Algorithms for Data Compression," \$3000, USF Sponsored Research, 1989.

BOOKS

1. **VLSI Algorithms and Architectures: Fundamentals**, edited by N. Ranganathan, IEEE Computer Society Press, June 1993.
2. **VLSI Algorithms and Architectures: Advanced Concepts**, edited by N. Ranganathan, IEEE Computer Society Press, June 1993.
3. **VLSI for Pattern Recognition and Artificial Intelligence**, edited by N. Ranganathan, World Scientific Publishing Co., April 1995.
4. S. Mohanty, N. Ranganathan, E. Kougiianos and P. Patra, **Low Power High Level Synthesis for Nanoscale CMOS Circuits**, Springer, Jan 2008.

BOOK CHAPTERS

1. N. Ranganathan and S. Henriques, "High Speed VLSI Designs for Lempel-Ziv based Data Compression", IEEE TCAS-II paper included in "High Performance VLSI Signal Processing - Innovative Architectures and Algorithms Vol I & II" edited by K.J. Ray Liu and K. Yao, IEEE Press, 1997.

2. N. Ranganathan and R. Venkataramana, "Integrated Circuits", invited article in 24-Volume Encyclopedia of Electrical Engineering, published by John Wiley and Sons, 1998.
3. M. Patel and N. Ranganathan, "A VLSI System for Intelligent Decision Making", invited chapter in "Neural Networks and Systolic Arrays", edited by D. Zhang and S.K. Pal, World Scientific Publishers, 2002.
4. S.Bhanja and N. Ranganathan, Hardware Implementation of Data Compression, in Lossless Compression Handbook, edited by K. Sayood, ISBN # 0-12-620861-1, Academic Press, 2003.

PATENTS

1. A Virtual Human Cadaver Navigation System, D. Hilbelink, N. Ranganathan and A. Loathe, U.S. Patent Application filed, 2006.
2. Method and Apparatus for Reducing Leakage in CMOS VLSI Circuits, U.S. Patent No. 7,256,608, Aug 2007.
3. High Speed VLSI Hardware for Lempel-Ziv Based Data Compression, U.S. Patent 5,179,378, Dec 1993.
4. Structure and Method for Dynamic Scene Analysis, U.S. Patent 5,604,821 Jan 1996.
5. VLSI Architectures for Polygon Recognition, U.S. Patent 5,535,292, July 1996, licenced by Intellectual Ventures Holding 10 LLC, 2007.
6. A VLSI Circuit Structure for Determining the Edit Distance Between Strings, U.S. Patent 5,553,272, Sept 1996.
7. A VLSI Circuit Structure for Implementing JPEG Image Compression Standard, U.S. Patent 5,659,362, Aug 1997 and International Patent allowed recently.

JOURNAL EDITORIAL ARTICLES

1. N. Ranganathan, Editorial: A Reflection on the TVLSI Editorial Process and the Announcement of a New Editor-In-Chief, IEEE Transactions on VLSI Systems, 15(1), Pp. 1-4, Jan 2007.
2. N. Ranganathan, Editorial: New Members of the Editorial Board, IEEE Transactions on VLSI Systems, 14(12), 1293-1294, Dec 2006.
3. N. Ranganathan, Editorial Appointments for 2005-2006 Term, IEEE Transactions on VLSI Systems, 13(7), Pp. 773-782, July 2005.
4. N. Ranganathan, Editorial: The Responsibility of Reviewers, IEEE Transactions on VLSI Systems, 12(12), pp. 1261-1262, Dec 2004.
5. N. Ranganathan, Editorial: Another Step in the Right Direction for TVLSI, IEEE Transactions on VLSI Systems, 12(7), Pp. 673, July 2004.
6. N. Ranganathan, Editorial, IEEE Transactions on VLSI systems, 12(1), Pp. 1-11, Jan 2004.

JOURNAL PUBLICATIONS

1. S. Bhattacharya, N. Ranganathan and S. Kim, A Framework For Correction of Multi-bit Soft Errors in L2 Caches Based on Redundancy, to appear in *IEEE Transactions on VLSI Systems*, 2008.
2. V. Mahalingam, N. Ranganathan and J. E. Harlow, "A Fuzzy Optimization Approach for Gate Sizing in the Presence of Process Variations", to appear in *IEEE Transactions on VLSI Systems*, 2008.
3. S.P. Mohanty and N. Ranganathan, "VLSI Architecture and Chip for Combined Invisible Robust and Fragile Watermarking", *IET Computers & Digital Techniques (Proceedings of IEE)*, 2007.
4. U. Gupta and N. Ranganathan, "Multi-Event Crisis Management Using Non-Cooperative Multi-Step Games", *IEEE Transactions on Computers*, 56(5), pages 1-13, May 2007.
5. N. Ranganathan, U. Gupta, R. Shetty and A.K. Murugavel, "An Automated Decision Support System Based on Game Theoretic Optimization for Emergency Management in Urban Environments", *Journal of Homeland Security and Emergency Management*, Berkeley Electronic Press, Pages 1-25, 2007 (Listed in Top 10 Downloaded Papers in the Journal).
6. K.P. Subbalakshmi, R. Chandramouli and N. Ranganathan, "A sequential distinguisher for covert channel identification," *International Journal of Network Security* , 5(3), pages 274-282, Nov 2007.
7. V. Mahalingam and N. Ranganathan, "Improving Accuracy in Mitchell's Logarithmic Multiplication using Operand Decomposition", *IEEE Transactions on Computers*, 55(12), Pages 1523-1535, Dec 2006.
8. N. Hanchate and N. Ranganathan, "Simultaneous Interconnect Delay and Crosstalk Noise Optimization through Gate Sizing Using Game Theory", *IEEE Transactions on Computers*, 55(8), Pages 1011-1023, Aug. 2006.
9. N. Hanchate and N. Ranganathan, "A Game Theoretic Framework for Multimetric Optimization of Interconnect Delay, Power and Crosstalk Noise During Wiresizing", *ACM Trans. on Design Automation of Electronic Systems*, 11(3), Pages 711-739, July 2006.
10. S. Bhanja, K. Lingasubramanian and N. Ranganathan, "A Stimulus-free Graphical Probabilistic Switching Model for Sequential Circuits using Dynamic Bayesian Networks", *ACM Transactions on Design Automation of Electronic Systems*, 11(3), Pages 773-796, July 2006.
11. S. P. Mohanty, N. Ranganathan, and S. K. Chappidi, "ILP Models for Simultaneous Energy and Transient Power Minimization during Behavioral Synthesis", *ACM Transactions on Design Automation of Electronic Systems* 11(1), Pages 186-212, Jan 2006.
12. S. P. Mohanty, N. Ranganathan, and K. Balakrishnan, "A Dual Voltage-Frequency VLSI Chip for Image Watermarking in DCT Domain", *IEEE Transactions on Circuits and Systems II (TCAS-II)*, Vol. 53, No. 5, Pages 394-398, May 2006.
13. S. P. Mohanty, N. Ranganathan, and R. K. Namballa, "A VLSI Architecture for Visible Watermarking in a Secure Still Digital Camera (S^2DC) Design", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 13, No. 8, August 2005, pp. 1002-1012.
14. S. P. Mohanty and N. Ranganathan, "Simultaneous Peak and Average Power Minimization during Datapath Scheduling", *IEEE Transactions on Circuits and Systems Part I (TCAS-I)*, Vol. 52, No. 6, June 2005, pp. 1157-1165.

15. S. P. Mohanty and N. Ranganathan, "Energy Efficient Datapath Scheduling using Multiple Voltages and Dynamic Clocking", *ACM Transactions on Design Automation of Electronic Systems*, 10(2), Pages 330-353, April 2005.
16. S. P. Mohanty and N. Ranganathan, "A Framework for Energy and Transient Power Reduction during Behavioral Synthesis", *IEEE Transactions on VLSI Systems*, 12(6), June 2004, pp. 562-572.
17. S. Bhanja and N. Ranganathan, "Cascaded Bayesian Inferencing for Switching Activity Estimation", *IEEE Transactions on VLSI Systems*, 12(12), Pages 1360-1370, Dec 2004.
18. A. Murugavel and N. Ranganathan, "A Game-Theoretic Approach for Power Optimization during Behavioral Synthesis", *IEEE Transactions on VLSI Systems*, 11(6), Pages 1031-1043, Dec 2003.
19. A. Murugavel and N. Ranganathan, "A Real Delay Switching Activity Simulator Based on Petri Net Modeling", *IEEE Transactions on VLSI Systems*, 11(5), Pages 921-927, October 2003.
20. S. Bhanja and N. Ranganathan, "Switching Activity Estimation of VLSI Circuits Using Bayesian Networks", *IEEE Transactions on VLSI Systems*, 11(4), Pp. 558-567, August 2003.
21. A. Ejnoui and N. Ranganathan, "Routing on Field Programmable Switch Matrices", *IEEE Transactions on VLSI Systems*, 11(2), Pp. 283-287, April 2003.
22. A. Ejnoui and N. Ranganathan, "Multi-terminal net routing for partial crossbar-based multi-FPGA systems", *IEEE Transactions on VLSI Systems*, 11(1), Pp. 71-78, Feb 2003.
23. R. Chandramouli, K.P. Subbalakshmi, and N. Ranganathan, "Channel-adaptive stochastic rate control for low bit rate wireless video transmission," Special issue on Video Objects: representation, creation, coding, transmission, manipulation and retrieval, *Pattern Recognition Letters*, 25(7), Pages 793-806, 2004.
24. N. Hanchate and N. Ranganathan, "LECTOR: A Novel Technique for Leakage Reduction in CMOS VLSI Circuits", *IEEE Transactions on VLSI Systems*, 12(2), Pages 196-205, Feb 2004.
25. A. Murugavel, N. Ranganathan, R. Chandramouli and S. Chavali, "Least Square Estimation of Average Power in Digital CMOS Circuits", *IEEE Transactions on VLSI Systems*, Vol. 10, No. 1, pp. 55-58, Feb 2002.
26. M. Patel and N. Ranganathan, "IDUTC: An Intelligent Decision Making System for Urban Traffic Control Applications", *IEEE Transactions on Vehicular Technology*, 50(3), Pp. 816-829, May 2001.
27. N. Ranganathan, M. Patel and R. Sathyamurthy, "An Intelligent System for Failure Detection and Control in Autonomous Underwater Vehicle," *IEEE Transactions on SMC*, i31(6), Pp. 762-767, Nov 2001.
28. A. Ejnoui and N. Ranganathan, "A partitioning algorithm for technology-mapped designs on single chip emulation systems", *IEEE Transactions on VLSI Systems*, Vol. 9, No. 2, April 2001, Pp. 407-410.
29. V.N. Ramaswamy, K. R. Namuduri and N. Ranganathan, "Context-based Lossless Image Coding using EZW Framework", *IEEE Transactions on Circuits and Systems for Video Technology (CSVT)*, 11(4), Pages 554-559, April 2001.
30. N. Vijaykrishnan and N. Ranganathan, "Object addressing support for a Java processor", *IEE Proceedings: Computers and Digital Techniques*, Nov 2000, Vol. 147, No. 6, pp. 435-443.

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89. V.N. Ramaswamy, K.R. Namuduri and N. Ranganathan, "Lossless Image Coding Using Wavelets and Variable Block Size Segmentation", Proc. of Intl. Symposium on Time-Frequency and Time-Scale Analysis, pp. 113-116, June 18-21, 1996, Paris, France.
90. M. Patel and N. Ranganathan, "A VLSI System Architecture for Intelligent Decision Making", Proc. of Intl. Conf. on Application Specific Array Processors, Chicago, 1996.
91. N. Ranganathan, S. Aruru and K.R. Namuduri, "A VLSI System Architecture for Lossless Image Compression", Proc. of Intl. Conf. on Pattern Recognition, ICPR, Aug 25-30, 1996.
92. K.R. Namuduri, N. Ranganathan and H. Rashedi, "SVBS: A High Resolution Medical Image Compression Scheme Using Slicing with Variable Block Size Segmentation" Proc. of Intl. Conf. on Pattern Recognition, ICPR 96, Aug 25-30, 1996.
93. S. Arumugavelu and N. Ranganathan, "SIMD Algorithms for Single Link and Complete Link Pattern Clustering", Proc. of Intl. Conf. on Pattern Recognition, Aug 25-30, 1996.
94. V.N. Ramaswamy, K.R. Namuduri and N. Ranganathan, "Lossless Image Compression Using Wavelet Decomposition", Proc. Intl. Conf. on Pattern Recognition, Aug 25-30, 1996.
95. N. Ranganathan, N. Vijaykrishnan and N. Bhavanishankar, "A Dynamic Frequency Linear Array Processor for Image Processing", Proc. of ICPR-96, Aug 25-30, 1996.

96. N. Ranganathan, S. Aruru and K.R. Namuduri, "A VLSI Chip for Image Compression Using Variable Block Size Segmentation", Proc. of Intl. Conf. on Computer Design, ICCD 96, Austin, pp. 500-505, Oct 1996.
97. N. Ranganathan, N. Vijaykrishnan and N. Bhavanishankar, "A VLSI Array Architecture with Dynamic Frequency Clocking", Proc. Intl. Conf. on Computer Design, Austin, pp. 137-140, Oct 1996.
98. N. Saxena, S. Sarkar and N. Ranganathan, "Mapping and Implementation of Bayesian Belief Networks on Hypercube", Proc. of Intl. Sym. on Parallel and Distributed Processing, SPDP'96, New Orleans, pp. 608-611, Oct 1996.
99. M. Patel and N. Ranganathan, "A VLSI System for Urban Traffic Control Applications", Proc. of Intl. Sym. on Parallel & Distributed Processing, SPDP, New Orleans, Oct 1996.
100. N. Ranganathan and R. Chandra, "A Systolic Algorithm and Architecture for Convex Bipartite Matching", Proc. of Intl. Conf. on High Performance Computing, HiPC'96, Trivandrum, Dec 18-22 1996.
101. M. Kovac and N. Ranganathan, "JAGUAR: A VLSI Architecture for Implementing JPEG Image Compression Standard", Proc. of Intl. Conf. on VLSI Design, New Delhi, Jan 1995, ** Best Paper Award Winner.
102. R. Sastry and N. Ranganathan, "A VLSI Architecture for Approximate Tree Matching," Proc. of Intl. Workshop on Parallel Processing, Bangalore, pp. 346-352, Dec 1994.
103. R. Sastry and N. Ranganathan, "A VLSI Architecture for Computing the Tree-to-Tree Distance," Proc. Intl. Symp. on High Perf. Comp. Arch.," Raleigh, NC, Jan 22-25, pp. 330-339, 1995.
104. M. Kovac and N. Ranganathan, "A Prototype VLSI chip for JPEG Image Compression Standard," Proc. IEEE EDAC-EUROASIC-95 Conference, Paris, Mar 6-9, 1995.
105. K.B. Doreswamy and N. Ranganathan, "A Systolic Algorithm and Architecture for Image Thinning", Proc. of Great Lakes Symposium on VLSI, pp. 138-143, March 1995.
106. N. Ranganathan, "Application Specific Parallel Architectures: Issues and Challenges", Invited Position Paper for Workshop on Challenges in Parallel Processing, Intl. Conf. on Parallel Processing, pp. 115-123, Aug 1995.
107. K.B. Doreswamy and N. Ranganathan, "A VLSI Chip for Computing the Medial Axis Transform of Images", Proc. of Computer Architectures for Machine Perception, CAMP 1995, Coma, Italy, pp. 36-43, Sept 1995.
108. A. Ejnioui and N. Ranganathan, "Systolic Algorithms for Tree Pattern Matching", Proc. of IEEE Intl. Conf. on Computer Design, ICCD'95, Austin, Oct 1-3, 1995.
109. A. Karimpuzha and N. Ranganathan, "A Systolic Algorithm and Architecture for Computing B-Splines and Bezier Curves", Proc. of Intl. Conf. on High Performance Computing, ICHPC, New Delhi, Dec 1995.
110. M. Kovac and N. Ranganathan, "ACE: A VLSI Chip for Galois Field Based Exponentiation," Proc. of Intl. Conf. on VLSI Design, Calcutta, India, pp. 291-296, Jan 5-8, 1994.
111. N. Ranganathan, B. Parthasarathy and K. Hughes, "A Parallel Algorithm and Architecture for Robot Path Planning," Proc. of Intl. Parallel Processing Symposium, Cancun, Mexico, April 1994 .

112. N. Ranganathan and S. Venugopal, "An Efficient VLSI Architecture for Image Template Matching," Proc. of International Conference on Parallel Processing, August 1994.
113. N. Ranganathan and S. Venugopal, "A VLSI Chip for Template Matching," Proc. of Intl. Conf. on Computer Design, ICCD '94, Boston, MA, pp. 542-545, October 1994.
114. N. Ranganathan, K.R. Namuduri and S. Romaniuk, "A Lossless Image Compression Algorithm Using Variable Block Size Segmentation," Proc. of Intl. Conf. on Pattern Recognition, Jerusalem, October 1994.
115. N. Ranganathan and S. Venugopal, "A VLSI Architecture for Template Matching Based on Moment Preserving Pattern Matching," Proc. of Intl. Conf. on Pattern Recognition, Jerusalem, October 1994.
116. N. Ranganathan, R. Sastry, R. Venkatesan, J. Yoder and D. Keezer, "SMAC: A Scene Matching Chip," Proc. IEEE Intl. Conference on Computer Design ICCD93, Cambridge, Massachusetts, pp. 171-180, October 1993.
117. R. Sastry and N. Ranganathan, "A VLSI Systolic Array for Approximate String Matching", Proc. IEEE Intl. Conference on Computer Design, ICCD93, Cambridge, MA, October 1993.
118. S. Kumar, N. Ranganathan and D. Goldgof, "Parallel Algorithms for Circle Detection on a Mesh-Connected Array of Processors," Proc. 8th Scandinavian Conf. on Image Analysis," Tromso, Norway, pp. 1019-1028, May 1993.
119. K. Hughes and N. Ranganathan, "A Model for Determining Sensor Confidence", Proc. IEEE Intl. Conference on Robotics and Automation, Atlanta, pp. 136-141, May 1993.
120. R. Sastry, N. Ranganathan, R.C. Jain, "VLSI Architectures for Depth Estimation using Intensity Gradient Analysis," Proc. of Intl. Parallel Processing Symposium, Newport Beach, California, pp. 700-704, April 13-16, 1993.
121. M. Kovac and N. Ranganathan, "Systolic VLSI Implementations of Galois Field Arithmetic Algorithms," Proc. IEEE EDAC-EUROASIC-93 Conference, Paris, February 22-25, 1993.
122. R. Sastry, N. Ranganathan and H. Bunke, "Hardware Algorithms for Polygon Matching," Sixth International Conference on VLSI Design, Bombay, India, Jan 4-8, pp. 41-44, 1993.
123. M. Kovac, N. Ranganathan and M. Varanasi, "SIGMA: A VLSI Chip for Galois Field Based Multiplication and Division," Proc. Sixth Intl. Conf. on VLSI Design, Bombay, Jan 4-8, pp. 25-30, 1993.
124. R. Sastry, N. Ranganathan and H. Bunke, "Systolic Architectures for Partial Polygon Recognition," Proc. IAPR Workshop on Structural and Syntactic Pattern Recognition, Bern, Switzerland, August 1992.
125. K. Hughes, A. Tokuta and N. Ranganathan, "TRULLA : An Algorithm for Path Planning Among Weighted Regions by Localized Propagations," Proc. Fifth Intl. Conference on Intelligent Robots and Systems, Iros', Raleigh, North Carolina, July 7-10, 1992.
126. A. Mukherjee, J. Flieder and N. Ranganathan, "MARVLE: A VLSI Chip for Variable Length Encoding and Decoding," Proc. IEEE Intl. Conference on Computer Design ICCD, Cambridge, Massachusetts, October 11-14, pp. 170-173, 1992.

127. M. Patel, P. McCabe and N. Ranganathan, "SIBA: A VLSI Chip for Image Processing," Proc. of International Conference on Pattern Recognition, The Hague, The Netherlands, August 1992, Vol. IV, pp. 15-18.
128. V.K. Sundaresan, S. Nichani, N. Ranganathan and R. Sankar, "A VLSI Hardware Accelerator for Dynamic Time Warping," Proc. of International Conference on Pattern Recognition, The Hague, The Netherlands, pp. 27-30, Vol. IV, August 1992.
129. R. Venkatesan, R. Sastry and N. Ranganathan, "A VLSI Architecture for Hierarchical Scene Matching," Proc. of International Conference on Pattern Recognition, The Hague, The Netherlands, pp. 214-217, August 1992.
130. K. Namuduri, R. Mehrotra and N. Ranganathan, "Edge Detection using Gabor Filters," Proc. of International Conference on Pattern Recognition, The Hague, The Netherlands, Vol. III, pp. 729-733, August 1992.
131. N. Ranganathan and K. R. Balaji, "A VLSI Chip for Attribute-based Relational Databases," Proc. International Conference on Information Systems and Management of Data, CISMODO, Bangalore, India, pp. 77-92, July 21-23, 1992.
132. M. Kovac, N. Ranganathan and M. Varanasi, "A Systolic Algorithm and Architecture for Galois Field Arithmetic," Proc. of Intl. Parallel Processing Symposium, Beverly Hills, California, pp. 283-288, March 23-25, 1992.
133. N. Ranganathan, S. Kurji and R. Mehrotra, "A CMOS VLSI Chip for Motion Detection," Proc. of Intl. Conference on VLSI Design, Bangalore, India, pp. 209-214, Jan 1992.
134. N. Ranganathan, Patrick McCabe and M. Patel, "A Programmable 2-dimensional Systolic Processor using 4-bit Processing Elements for Image Processing," Proc. of Intl. Conference on VLSI Design, Bangalore, India, pp. 215-220, Jan 1992.
135. S. Nichani and N. Ranganathan, "Design of a High Speed VLSI Chip for Scale Space Computation," Proc. of SPIE Conference on Applications of Artificial Intelligence X : Machine Vision and Robotics, Orlando, April 20-24, 1992.
136. N. Ranganathan, R. Mehrotra and S. Subramaniam, "A High Speed Systolic Architecture for Labeling Connected Components in an Image," Proc. IEEE International Symposium on Parallel and Distributed Processing, Dallas, Texas, pp. 818-825, December 1-5, 1991.
137. K. Chaudhury, R. Mehrotra and N. Ranganathan, "A Parallel Algorithm for 3-D Point Pattern Matching," Proc. IEEE Intl. Conference on Systems, Man and Cybernetics, Charlottesville, Virginia, pp. 105-111, Oct. 13-16, 1991.
138. N. Ranganathan and S. Henriques, "A Systolic Architecture for LZ-based Decompression," Proc. of Data Compression Conference, Snowbird, Utah, pp. 450-451, April 8-11, 1991.
139. N. Ranganathan and S. Henriques, "A Systolic VLSI Chip for Data Compression," Proc. IEEE International Symposium on VLSI Design, New Delhi, pp. 310-311, Jan 4-8, 1991.
140. N. Ranganathan, K. Namuduri and R. Mehrotra, "An Architecture to Implement Multiresolution," Proc. of IEEE Intl. Conf. on ASSP, Toronto, Canada, May 14-17, pp. 1157-1160, 1991.

141. S. Henriques and N. Ranganathan, "A Parallel Architecture for LZ-based Data Compression," Proc. IEEE Intl. Symposium on Parallel and Distributed Processing, Dallas, pp. 262-266, Dec 9-13, 1990.
142. S. Nichani and N. Ranganathan, "SAP: Design of a Systolic Array Processor for Computations in Vision," Proc. IEEE International Conference on Computer Design, ICCD '90, Cambridge, MA, pp. 315-318, September 17-19, 1990.
143. K. Namuduri, R. Mehrotra and N. Ranganathan, "Fast Spatiotemporal Filters," Proc. 10th Intl. Conference on Pattern Recognition, Atlantic City, pp. 479-483, June 16-21, 1990.
144. N. Ranganathan and R. Mehrotra, "A VLSI Architecture for Dynamic Scene Analysis," Proc. 10th Intl. Conf. on Pattern Recognition, Atlantic City, pp. 506-508, June 16-21, 1990.
145. N. Ranganathan and H. N. Srinidhi, "Effect of Data Compression Hardware on the Performance of a Relational Database Machine," Proc. IEEE Intl. Conf. on Parallel Architectures & Databases (PARBASE '90), Miami, pp.144-146, March 7-9, 1990.
146. N. Ranganathan, S. Nichani and R. Mehrotra, "A VLSI Architecture for Corner Detection," Proc. Intl. Work. on Algorithms & Parallel VLSI Architectures, France, June 10-16, 1990.
147. N. Ranganathan, S. Subramanian and R. Mehrotra, "A High Speed VLSI Architecture for Connected Component Labeling," Proc. Intl. Workshop on Algorithms and Parallel VLSI Architectures, France, June 10-16, 1990.
148. N. Ranganathan and R. Mehrotra, "A VLSI Based System for Motion Analysis in Scene Images," Proc. IEEE Intl. Conf. on Tools for AI, Fairfax, VA, pp. 592-597, Oct 23-25, 1989.
149. A. Mukherjee, N. Ranganathan and M. Bassiouni, "Adaptive and Pipelined VLSI Designs for Tree-based Codes," Proc. IEEE Intl. Conf. on Computer Design (ICCD '89), Cambridge, Massachusetts, pp. 369-373, Oct. 2-4, 1989.
150. A. Mukherjee, N. Ranganathan and M. Bassiouni, "On Software and Hardware Techniques of Data Encoding," Proc. of Fifth Intl. Conf. on Data Engineering, Los Angeles, pp. 208-215, Feb. 6-10, 1989.
151. N. Ranganathan and M. Shah, "A Scale Space Chip," Proceedings of 9th International Conference on Pattern Recognition, Roma, Italy, pp. 420-424, Nov. 14-18, 1988.
152. A. Mukherjee, N. Ranganathan and M. Bassiouni, "High Speed VLSI Encoding Chips for Supercomputers," Proc. of 3rd Intl. Conf. on Supercomputing, Boston, May 15-20, 1988.
153. A. Mukherjee, M. Bassiouni and N. Ranganathan, "Improving Bandwidth of Communication Controllers," Proc. of IEEE Intl. Conf. on Communications (ICC 88), Philadelphia, pp. 1390-1394, June 12-15, 1988.
154. M. Bassiouni, N. Ranganathan and A. Mukherjee, "Software and Hardware Enhancement of Arithmetic Coding," Proc. of 4th Int. Conf. on SSDBM, Roma, Italy, pp. 120-132, June 21-23, 1988.
155. M. Bassiouni, N. Ranganathan and A. Mukherjee, "A Scheme for Data Compression in Supercomputers," Proc. of Supercomputing 88, Orlando, pp. 272-278, Nov. 14-18, 1988.

MANUSCRIPTS IN PREPARATION/SUBMITTED

1. U. Gupta and N. Ranganathan, ""A Micro-Economic Approach for Multi-Objective Clustering", IEEE Transactions on Computers, to be submitted, Jan 2007.

2. A. K. Murugavel and N. Ranganathan, "Low power techniques for gate sizing and buffer insertion during logic synthesis", IEEE Trans. on VLSI Ssystems, in review.
3. S. P. Mohanty and N. Ranganathan, Low power system design using voltage-frequency reduction : A survey, Journal manuscript under preparation.
4. N. Ranganathan, A. Ejnoui and K. Sitaraman, "A VLSI System Architecture for Object Recognition in Scene Images", IEEE Transactions on Circuits and Systems for Video Technology.
5. R. Venkataramana and N. Ranganathan, "A Learning Automaton Based Framework for Task Partitioning and Scheduling with Multiple Costs in Heterogenous Computing Systems", IEEE Transactions on Parallel and Distributed Systems.
6. N. Ranganathan and S. Venugopal, "A VLSI Chip for Moment Preserving Pattern Matching", in preparation for IEEE Transactions on Video Technology.
7. N. Ranganathan, R. Anand and G. Chiruvolu, "A VLSI ATM Switch Architecture for VBR Traffic", IEEE Transactions on VLSI Systems.

VLSI CHIPS DESIGNED/SUPERVISED

1. Design of an nMOS Pipeline Wallace Multiplier Chip, 1984.
2. Design of an nMOS chip for Polygonal Mask Generation, 1985.
3. Design of a Prototype CMOS Chip for Huffman-based Data Compression, 1987.
4. Design of a Systolic Array Processor Chip for Scale Space Computation, 1989.
5. Design of a Systolic Array CMOS Chip for LZ-based Data Compression, 1990.
6. Design of a Run-length Based Compression CMOS Chip, 1990.
7. Design of SIGMA: Systolic Chip for Galois Field-based Multiply/Divide, 1990.
8. Design of a Prototype CMOS Chip for Huffman-based Decompression, 1990.
9. Design of a Systolic CMOS Chip for Join Computation in RDBMS Systems, 1991.
10. Design of a Systolic Array Processor CMOS Chip for Dynamic Scene Analysis, 1991.
11. Design of a 2-D Systolic Array processor CMOS Chip for Image Processing, 1991.
12. Design of a Memory-based CMOS VLSI Chip for JPEG Baseline Compression, 1991.
13. Design of a CMOS VLSI Chip for Hierarchical Scene Matching, 1992.
14. Design of a CMOS VLSI Chip for Approximate String Matching, 1993.
15. Design of a CMOS VLSI Chip for Polygon Recognition, 1993.
16. Design of a CMOS VLSI Chip for Approximate Tree Matching, 1994.
17. Design of a CMOS VLSI Chip for Template Matching, 1994.

18. Design of a CMOS VLSI Chip for JPEG Image Compression Standard, 1994.
19. Design of a CMOS VLSI Chip for Image Thinning, 1995.
20. Design of a CMOS VLSI Chip for Tree Pattern Matching, 1995.
21. Design of a CMOS VLSI Chip for Intelligent Decision Making, 1995.
22. Design of a CMOS linear Array Processor with Variable Rate Clocking, 1995.
23. Design of a CMOS VLSI Chip for Maximal Matching in Bipartite Graphs, 1995.
24. Design of a Chip for Image Compression with Variable Size Segmentation, 1995.
25. Design of a Chip for Contiguous Binary String Matching CBS Problem, 1995.
26. Design of a CMOS VLSI Chip for Tree Matching, 1996.
27. Design of a CMOS Chip for Connected Component Labeling, 1996.
28. Design of a CMOS Chip for Cancer Detection using Digital Mamograms, 1996.
29. Design of a CMOS VLSI ATM Switch Prototype, 1997.
30. Design of a CMOS VLSI Chip for Motion Estimation from Video, 1998.
31. Design of a CMOS VLSI Chip for Object Recognition in Images, 2002.
32. Design of a CMOS VLSI Chip for Invisible Digital Image Watermarking, 2003.
33. Design of a CMOS VLSI Chip for Visible Digital Image Watermarking, 2003.
34. Design of a Dual Voltage-Frequency Chip for Watermarking in DCT Domain, 2004.

INVITED TALKS

1. "Graduate Education in U.S. Universities", Regional Engineering College, Tiruchi, July 1985.
2. "Data Compression", Indian Institute of Technology, Madras, India, June 1988.
3. "Higher Education in Engineering", St. Peter's High School, Tanjore, June 1988.
4. "Data Compression Hardware", IEEE and ACM Tampa Bay Section, October 1988.
5. "VLSI Design", Regional Engineering College, University of Madras, July 1989.
6. "VLSI Algorithms and Architectures", IIT-Madras and IEEE Madras Section, Dec 1990.
7. "Performance in Very Large Databases", K.J. Somaiya Institute, Bombay, Jan 1992.
8. "VLSI for Data Compression," University of Central Florida CS Colloquium, Sept. 23, 1992.
9. "VLSI Hardware for Data Compression," ACM/IEEE Tampa Bay Section, Nov 18, 1992.
10. Data Compression, East Tenn. State Uni. ACM chapter, Johnson City, TN, Nov 1993.
11. Data Compression, IIT, Bombay, IEEE DVP Speaker, Dec 1995.

12. VLSI For Pattern Matching, UCF, Orlando, April 1997.
13. Application Specific VLSI Systems, Uni. of Houston, April 1997.
14. Lossless Data Compression, ITEM University, Cuernavaca, October 1997.
15. Image Transmission over Wireless Channels, UCF, Orlando, IEEE DVP Speaker, Nov 1997.
16. Application Specific VLSI Systems, Uni. of Texas at El Paso, Feb 1998.
17. VLSI Systems for Data Compression, SVCE College of Eng., Uni. of Madras, May 1998.
18. Power Estimation and Optimization, Distinguished Speaker Lecture Series, Cadence Inc., Boston, September 2002.
19. ASICS as a Solution to Biomechanics, Invited Keynote address in Intl. Conf. on Biomechanics, April, 2004.
20. Impact of VLSI Technology on Future Computing, I2IT, Pune, India, Aug 2004.
21. Game Theoretic Optimization for Interconnect Design, Tata Consultancy Services, Bangalore, 2006.
22. Multimetric Optimization in VLSI CAD, Invited Keynote Address in Intl. Conf. on Brain Modeling and Supercomputing, 2007.
23. VLSI Technology and Its Future, Meenakshi College, Chennai, 2007.
24. Game Theory in VLSI CAD, Texas Instruments Bangalore, 2007.
25. Multimetric Challenges in Nanoscale Computer Design, USF University Lecture Series, 2007.
26. Invited Panel Speaker, VLSI Education in US Universities, Intl. Student Conf. on VLSI Design, hosted by VEDA-IIT, Hyderabad, 2008.
27. Multimetric Challenges in VLSI Design, EE Dept., IIT-Madras, 2008.

PH.D. DISSERTATION GUIDANCE AS MAJOR PROFESSOR

1. K. V. Namuduri, Gabor Filter Based Models for Low-level Vision, Sept 1992; Associate Professor, Wichita State University, Kansas; previously at CTSPS, Clark Atlanta University, Atlanta, GA.
2. K. Hughes, Multi-sensor Based Confidence Measurement Model for Robot Path Planning, May 1994; Faculty, Dept. of ECE, Uni. of Pacific, Stockton, CA.
3. R. Sastry, VLSI Architectures for Pattern Matching and Recognition, Aug 94; Senior Member of Technical Staff, PMC-Sierra, previously with Fujitsu HaL, Agilent Labs and Redswitch Inc., Campbell, CA; **USF Graduate Council Outstanding Dissertation Award & SIGMA CHI Outstanding Dissertation Award.**
4. M. Patel, RAPID: A Real-Time System for Intelligent Decision Making, Aug 1997; Senior Systems Engineer, Satellite and Advanced Processing Avionics, Honeywell Space Systems, Clearwater, FL.
5. G. Chiruvolu, Efficient Transportation of VBR Video Traffic in ATM Networks, April 1998; Research Scientist, Alcatel, Richardson, TX.

6. V. Ramaswamy, Lossless Image Compression Using Wavelet Decomposition, April 1998; Member of Technical Staff, Bell Laboratories, Holmdel, NJ.
7. N. Vijaykrishnan, "Issues in the Design of a Java Processor", July 1998; Associate Professor, Dept. of CSE, Penn State University, Univeristy Park, PA.
8. V. Krishna, High Level Techniques for Power Estimation, Analysis and Optimization, Jan 1999; Senior Member of Technical Staff, Agilent Research Labs, Palo Alto; **USF Graduate Council Outstanding Dissertation Award.**
9. R. Chandramouli, Theory and Application of Sequential Detection under Dependence, Jan 1999; Assistant Professor, Dept. of ECE, Iowa State University; Stevens Inst. of Technology, NJ; **USF Graduate Council Outstanding Dissertation Award.**
10. H. Oi, Bidirectional Ring Based Multiprocessor, Nov 1999, Senior Architect, HaL Computer Systems, joining FAU as faculty in 2001.
11. A. Ejnoui, Routing and Partitioning in FPGA-based Emulation Systems, August 1999; Assistant Professor, School of EECS, Uni. of Central Florida, 2001.
12. R. Venkatramana, Partitioning and Scheduling for Heterogenous Computing Systems, May 2000, Senior Design Engineer, Honeywell Inc., Clearwater, FL.
13. S. Bhanja, Power Estimation in CMOS Circuits Using Bayesian Networks, July 2002, Assistant Professor, Uni. of South Florida, Dept of EE.
14. A. Murugavel, Power Estimation and Optimization in CMOS VLSI Circuits, August 2003, Senior CAD Engineer, Intel Corporation, Hillsborough, Oregon. **SIGMA XI Tampa Bay Chapter Outstanding Dissertation Award and the USF Graduate Council Outstanding Dissertation Award.**
15. S. P. Mohanty, High Level Synthesis of Low Power High Performance Datapath Designs, graduated Dec 2003; Assistant Professor, Uni. of North Texas, Denton.
16. V. Sairaman, Low Power High Performance Embedded Systems, Phd Candidate, May 2008, expected.
17. N. Hanchate, Leakage Power Analysis and Optimization, graduated May 2006, Senior CAD Engineer, Synopsys, San Jose, CA.
18. K. Rojas, Hardware and Software for SKIN Interface, IGERT Phd Fellow, jointly with Dr. R. Sankar, EE.
19. U. Gupta, Multimetric Optimization Using Game Theory, Phd Candidate.
20. V. Mahalingam, Modeling Process Variations for VLSI Circuit Optimization, Phd Candidate.
21. Elizabeth Horton, VLSI Hardware for Bioinformatics, IGERT Phd Candidate.
22. S. Roy, An Integrated Framework for Powergating in Microprocessor Systems, Ph.d. candidate, co-major professor jointly with Dr. S. Katkoori.
23. A. Oruganti, VLSI Design Automation, Phd candidate.
24. K. Bhattacharya, Soft Errors and Variability Optimization in System Design, Ph.d. candidate.
25. Ransford Hyman Jr., VLSI Design Automation, Ph.D. Student, Bridges to the Doctorate Program.

26. H. Thaplial, Reversible Logic Based FPGA Design, Phd Student.
27. D. Srinivasan, Mapping Applications to Multi-core Architectures, Phd Student.

M.S. THESIS GUIDANCE AS MAJOR PROFESSOR

1. Sanjay J. Nichani, "SAP: Systolic Array Processor for Computations in Vision", April 1990.
2. Suresh Subramanian, "VLSI Algorithms for Connected Components Labeling", April 1990.
3. Selwyn Henriques, "SALCOM: Systolic Architecture for LZ Data Compression", Dec 1990.
4. Elizabeth Meyer, "A CMOS VLSI Chip for Huffman-based Decompression", April 1991.
5. Balaji, K. R., "A Systolic Chip for Computation of Join in Relational Databases", Dec 1991.
6. V.K. Sundaresan, "Software and Hardware Solutions for Dynamic Time Warping", Dec 1991.
7. R. Nyapathi, "Hypotheses-based Object Recognition", Dec 1991.
8. Pat McCabe, "A 2-D Systolic Array Architecture for Image and Signal Processing", May 1992.
9. Minesh Patel, "Design of a 2-D VLSI Systolic Array Chip for Image Processing", May 1992.
10. Jeffrey Fleider, "A VLSI Chip for JPEG Baseline Compression/Decompression", May 1992.
11. Raghuveer Venkatesan, "VLSI Architectures for Hierarchical Scene Matching," Aug 1992.
12. Michael Sullivan, "Systolic VLSI Designs for Data Compression", May 1992.
13. Shamira Kurji, "A VLSI Chip for Motion Detection".
14. K. Remedios, "A VLSI Chip for Approximate String Matching", July 1993.
15. B. Parthasarathy, "A VLSI Architecture for Robot Path Planning," October 1993.
16. S. Venugopal - "A VLSI Architecture for Template Matching," April 1994.
17. A. Karimpuzha - "VLSI Architectures for Curve Generation," July 1995.
18. V. Natarajan - "VLSI Architectures for Data Compression,".
19. B. D. Kiran - "VLSI Architectures for Image Thinning", April 1995.
20. A. Ejnoui, "Parallel Algorithms for Tree Pattern Matching", March 1995.
21. R. Motamarri - "VLSI Architecture for CBS Matching", December 1995.
22. N. Saxena - "Implementation of Bayesian Networks on Hypercube", Dec 1995.
23. V. Krishna - "VLSI Chip for Tree Pattern Matching", April 1996.
24. S. Aruru - "VLSI Chip for Image Compression with Variable Block Segmentation", Dec 1995.
25. P. Solarzano - "FPGA Implementation of LZW Compression for Modems".
26. H. Rashedi - "Lossless Compression of Digital Mammogram Images", December 1995.

27. S. Shivaraman - "Joint Source and Channel Coding", August 1996.
28. Weyron Henriques - "VLSI System for Enhancement of Digital Mammograms", Oct 1996.
29. V. Sundaram - "3-D Volumetric Medical Data Compression", September 1996.
30. A. Konduru - "A Compression Algorithm for Relational Databases", Dec 1997.
31. R. Sathyamurthy, "Intelligent Decision Making for Underwater Navigation", Apr 1996.
32. R. Chandra, "A VLSI Chip for Maximal matching in Bipartite Graphs", February 1996.
33. N. Bhavanishankar, "A VLSI Chip for Image Processing", April 1996.
34. A. Rasquinha, "A Connected Component Labeling Chip & FPGA Implementation", Sept 1996.
35. R. Margapur, "A VLSI System for Neural Network Implementation".
36. R. Venkataramana, "A VLSI Hardware Router for MIMD Systems", Aug 1997.
37. R. Anand, "A VLSI Chip for Buffer Allocation & Management in ATM Networks", May 1997.
38. P. Singh, "A new DCT Algorithm and its VLSI Architecture for MPEG-II Audio Layer Standard", May 1997.
39. S. Crasta, "A New Algorithm for Lossless Compression of Text Databases", Dec 1997.
40. R. Gadekarla, "A New Profiling Tool for JAVA Execution", Dec 1997.
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