CAREER: Performance Evaluation of Gigabit Ethernet Networks,
a Systems and Experimental Approach

Kenneth J. Christensen
Department of Computer Science and Engineering
University of South Florida
Tampa, Florida 33620
Phone: (813) 974-4761
Email: christen@csee.usf.edu
PROJECT SUMMARY

Research Plan

It is evident that both ATM and Ethernet networks will comprise the “network of the future”. Ethernet networks are rapidly transitioning from half-duplex CSMA/CD to full-duplex switched operation. While much of the current research in ATM networks is relevant to both types of networks, there are significant remaining problems in the area of Ethernet networks that urgently need to be addressed. These problems include:

1. The traffic characteristics of future gigabit applications have not yet been predicted. Current traffic models may not be applicable for gigabit applications. Therefore, better knowledge of traffic from expected gigabit applications is needed to be able to predict network performance.
2. For high-speed networks, memory speed limits output buffered and shared memory switch architectures to low port densities. For this reason, scheduling algorithms which achieve high throughputs for input buffered only ATM switches have been the subject of recent research. Yet, there do not exist scheduling algorithms or switch architectures which accommodate variable length packets and Quality of Service (QoS) in input buffered only switches and full-duplex repeaters.
3. While switched operation will likely be predominant in future networks, inefficiencies in gigabit half-duplex CSMA/CD Ethernet still remain and need to be addressed.

The objective of this four year CAREER program is to address these problems. Existing traffic models are largely based on time series analysis of traffic traces resulting in a limited understanding of the causes of observed traffic characteristics. New knowledge will be gained by instrumenting application and protocol implementations to study the user behavior, source data objects, and application and protocol behaviors of expected gigabit applications. Using the resulting traffic models as input to performance models that will be developed, methods for highly scalable, input buffered only switches to provide high throughput and efficient support for bursty, best-effort data traffic and guaranteed-service traffic streams will be advanced. The hypothesis is that by using traffic shaping at each input port, the scheduling algorithm can be made simple and scalable. The applicability of packet bursting and spacing, priority queueing, and selective PAUSE flow control will be studied. To support CSMA/CD on large span, half-duplex Gigabit Ethernet networks with high-data rates, the current minimum 64-byte packet size must effectively be increased to 512 bytes to allow for correct collision detection. The IEEE 802.3 Gigabit Ethernet standard uses packet bursting to transmit small packets. A more efficient and interoperable method of operation whereby late collisions are permitted, can be detected, and handled correctly will be studied.

A systems and experimental approach will be used to tackle the problems. A laboratory of Gigabit Ethernet attached personal computers and servers will be built. This laboratory will be used for direct experimentation, as a facility for parallel execution of simulation models, and for related educational activities at both the graduate and undergraduate levels. A tool for parallel independent replications of simulation models will be developed and made generally available. Much more significantly, new ideas in traffic modeling, new knowledge in switch scheduling for variable length packets with support for QoS, and new methods for using CSMA/CD in large span, half-duplex Ethernet networks will be presented in appropriate conferences and journals, and to standards bodies. To solicit input and generate external participation, a WWW site with a bulletin board will be established for researchers and developers from academia and industry to share software tools, new ideas, and findings. In addition, a workshop will be held. New ideas will thus be seeded into the research community.

Education Plan

The College of Engineering at the University of South Florida currently has a new undergraduate degree track in Information Systems. A graduate track in Information Systems is under consideration. This CAREER program will advance a strong networking and performance modeling focus for this Information Systems degree track. New courses and curricula will be developed and research results will be brought into the classroom. The emphasis will be on experimental and hands-on projects where students will work in teams to solve real world problems using cutting-edge knowledge. The educational materials developed as a result of this project will be used as a contribution to ongoing ACM and IEEE-CS efforts to develop curriculum guidelines for Information Systems programs. To encourage undergraduate students to pursue graduate education in engineering, portions of this CAREER program have been explicitly identified for undergraduate student research involvement.
PROJECT DESCRIPTION

1. Introduction and Problem Statement

This 1998 NSF CAREER proposal addresses significant research problems in the area of high-speed networks with an emphasis on Gigabit Ethernet networks. ATM and Ethernet networks are both becoming the “network of the future”, with Ethernet networks playing a major role as an edge network. It is unreasonable to assume that either ATM or Ethernet will entirely dominate, hence research is needed in areas related to both types of networks. Emerging Gigabit Ethernet (see [31]) supports both half-duplex CSMA/CD and full-duplex repeated and switched access. There exist open problems in the area of Gigabit Ethernet that urgently need to be addressed. Three of these urgent problems that will be addressed in this four-year CAREER program are:

1. The traffic characteristics of future gigabit applications have not yet been predicted. Current traffic models may not be applicable for gigabit applications. Better knowledge of traffic from expected gigabit applications is needed to be able to predict network performance. For example, what are the expected characteristics of image retrieval, WWW server clustering, network caching for data-intensive computing applications, and high-definition video delivery?

2. For high-speed networks, memory speed limits output buffered and shared memory switch architectures to low port densities. Recent work (see [47]) demonstrates that with parallel-queue input buffers and suitable input-output matching algorithms, output buffers are not needed to achieve high throughput in an ATM switch. Can these algorithms be extended to input buffered only switches and repeaters that use variable length packets? In addition, can new methods be advanced to support simultaneous bursty, best-effort data traffic and guaranteed-service traffic streams (i.e., QoS) in these switches and repeaters?

3. While switched operation will likely be predominant in future networks, inefficiencies in gigabit half-duplex CMSA/CD Ethernet still remain and need to be addressed. Simple carrier extension (from [27]) can result in a Gigabit Ethernet throughput barely greater than that of 100-Mbps Ethernet (see [51]). Packet bursting (see [52]) may not be much better in some cases. How can small packets be efficiently supported in a half-duplex Ethernet where the network round-trip delay exceeds the transmission time of a small packet?

The above three research problems are related. Without knowledge of traffic, especially knowledge of source-destination correlations in bursts of packets, performance of network components such as switches cannot be evaluated. Input buffered only switches, long thought as impractical due to Head-of-Line (HOL) blocking effects, are currently at the forefront of research (see, for example, [47]). Input-output matching algorithms and new buffer configurations are reducing HOL effects, however very little work has been done to enable input buffered only switch architectures to support QoS. The full-duplex repeater for Gigabit Ethernet (see [21]) can be considered as a type of an input buffered switch with a switching scale-up of one. While most modern network media and physical topologies support full-duplex operation, research in half-duplex operation is not without merit. For very high-speeds where physical layer costs dominate (or where cabling plants best support half-duplex baseband operation), half-duplex multiple access networks may hold an economic advantage over fully-switched, full-duplex networks and should therefore be studied. In an NSF funded workshop (see [57]) the need for continued research in shared media access technologies was noted, in addition to the need for research in switching technologies, efficient interfacing of computers to Gigabit networks, and improved protocols.

Education in the area of computer networks is largely limited to a technology course, (e.g., based on [66]) or a TCP/IP programming course (e.g., based on [18]). Little emphasis is placed on experimental projects or on the quantitative aspects of network analysis and design. The latter is especially true at the undergraduate level. This CAREER program will bring research results, tools, and laboratory equipment into the classroom. In addition, research opportunities for advanced undergraduate students will be made available. The complete education plan showing a linkage of research and teaching is presented after the research plan in this program description.

The remainder of this program description is organized as follows. Section 2 describes the objectives, scope, and significance of this program. Section 3 is a background review of relevant existing research in the three problem areas. Section 4 is a research plan that describes the methods to be used. Section 5 is an education plan and describes course and curriculum contributions to be made to the Information Systems degree track at the University of South Florida. As appropriate to a CAREER proposal, Sections 3 and 5 also include descriptions of accomplishments by the principal investigator. Section 6 is a four-year overall program plan describing yearly activities and expected outcomes and benefits. Finally, Section 7 is the departmental endorsement.
2. Objectives, Scope, and Significance

The objectives of this four year CAREER program are to solve research problems confronting high-speed networks and in particular Gigabit Ethernet networks, build a community of researchers to focus on these and other problems, and contribute directly to course and curriculum development in the area of Information Systems. In addition, useful performance modeling and simulation tools will be developed and made generally available. The measurable objectives corresponding to the three specific problems described in the previous section are:

1. Characterize traffic from representative gigabit applications. Analyze the user behavior, data object characteristics, and application and protocol behaviors. Develop empirical traffic models (similar, for example, to tcplib in [22] and SURGE in [3]) useful for the further study of these applications.

2. Advance new algorithms for achieving high throughput in input-buffered only Ethernet switches and full-duplex repeaters. Study the application of traffic shaping and scheduling algorithms to enable QoS support in input buffered only switches. Demonstrate that these methods can be used to provide simultaneous best-effort and guaranteed-service in switched and repeated Gigabit Ethernet.

3. Propose and study a backwards-compatible CSMA method, called CSMA with Timed Collision Detection (CSMA/TCD), that allows for late collision detection and handling in large-span, half-duplex Ethernet. The CSMA/TCD method will be compared to the existing IEEE 802.3 packet bursting method (see [52]) and is expected to offer higher network utilization (than packet bursting).

This CAREER program promotes a systems and experimental approach to research in very high speed networks. Problem (1) involves experimental laboratory work in instrumenting application and protocol implementations and in collecting traffic traces. Problems (2) and (3) are performance modeling problems entailing experimental, simulation, and analytic approaches.

The significance of this CAREER program extends to the research, industry, and education communities. New traffic models and traffic characterization methods can directly benefit many other researchers studying high-speed networks. New switch scheduling algorithms and architectures for Gigabit Ethernet can directly benefit both researchers and practitioners. By offering backward compatible solutions to “standardized” problems, contributions can be made to the IEEE 802.3 even after an expected 1998 standardization of Gigabit Ethernet. This CAREER program will support the education of the next-generation network practitioners and researchers within the scope of Information Systems. Information Systems as an independent field of study addresses both the theoretical and practical aspects of specifying, designing, implementing, and managing information systems. This CAREER program will contribute towards the curriculum development of Information Systems by developing new courses in the core areas of computer networking and performance evaluation. In the long term, this CAREER program will bring a serious research and education focus to switched Ethernet networks, something that is currently lacking.

3. Background Review for Research

This section contains a review of applicable work in 1) traffic modeling, 2) input buffered switching including QoS scheduling, Gigabit Ethernet Full-Duplex Repeaters (FDR), and PAUSE flow control, and 3) performance of half-duplex, CSMA/CD Gigabit Ethernet. This section begins with a description of the principal investigator’s research accomplishments.

3.1 Description of research accomplishments by the principal investigator

The principal investigator joined the faculty at the University of South Florida as an Assistant Professor in August 1995, following a 10-year career at IBM Corporation in the Research Triangle Park, North Carolina. While at IBM, the principal investigator earned eight patents pertaining to improvements to LAN switching, see [20]. The first two years of the principal investigator’s academic career were largely focused on performance modeling of the Binary Logarithmic Access Method (BLAM). BLAM is a proposed IEEE 802.3 Ethernet standard (proposed by Mart Molle, see [49] and [25]). The principal investigator developed the first independent simulation model of BLAM with initial results published in [8] and [9] and also presented to the IEEE 802.3w task force in March 1996. The simulation model is based on a unique “station-centric” approach (see [16]) that allows for very accurate modeling of heterogeneous host (station) types and traffic sources. In [50] the BLAM simulation model is used to repeat the classic Ethernet multimedia performance study from [69] and it is shown how a BLAM Ethernet can support significantly greater numbers of video streams than can a standard Binary Exponential Backoff (BEB) Ethernet. The third year
focused on modeling the Gigabit Ethernet full-duplex repeater and switched Ethernet (see [15]). The Gigabit full-duplex repeater was shown to perform significantly better than half-duplex CSMA/CD with packet bursting. For the summer of 1998 the principal investigator was awarded an NASA/ASEE fellowship and is studying performance evaluation methods to be used for validating designs of future NASA-KSC networks.

Other research accomplishments (including those completed in association with M.S. and Ph.D. students and IBM partners as listed in the publication author lists) are:

- A model and prediction of Hypertext Transfer Protocol (HTTP) performance for HTTP 1.1 in [14].
- Exact analysis of ATM cell probabilities in switch buffers given periodic on/off traffic in [61].
- A method of reducing traffic self-similarity by application-level source control in [10].
- A method for maintaining connections for power-managed client computers in [13].
- Efficient computation of packet CRC’s from partial CRC’s with application to ATM CIF in [60].
- Use of Tabu search to find optimal switch LAN configurations in [54].
- Reduction of ATM CAC overhead by utilizing aggregated traffic statistics in [65].
- Adaptive sampling methods for traffic characterization (including the Hurst parameter) in [24].
- Use of selective discard to improve real-time video quality on CSMA/CD Ethernet in [44].

This CAREER program intends to build on these research accomplishments and established relationships.

### 3.2 Traffic modeling for gigabit applications

Traditional traffic modeling relies on time series analysis of network traffic traces and the fitting of probability distributions to these traces. These fitted probability distributions can be as simple as single parameter Poisson distributions, or more complex multiple parameter models involving both short and long range correlations. The seminal work in LAN traffic analysis is [32] and is also one of relatively few studies to look at source-destination correlations within packet bursts. In [39] network traffic was first shown to possess properties of long range dependence, making the use of Poisson models for even highly aggregated traffic a poor fit. The study in [58] further demonstrates that network traffic is not Poisson, except in the case of terminal connection interarrival times made by independent human telnet users. Other traffic studies, including [4] for video traffic and [19] for WWW traffic, show that network traffic of many different types is self-similar and have thus begun to raise questions on why and how these and other statistical properties occur. Heavy-tailed properties of distributions of user behavior and data objects may be at the root of self similarity of network traffic (see [28]). Figure 1 shows the measured distribution of call hold times for the PPP modem pool at the University of South Florida used for dial-in Internet access by students. The figure shows the results of two weeks of data collection at the dial-in service router. For a collected 181,770 samples, the mean call hold time is 24.6 minutes. Comparing the measured USF PPP to a simulated exponential distribution with the same mean hold time and number of samples clearly demonstrates the heavy tailed property of the PPP call hold times. Similar heavy tailed results (not shown here) have been found in the distribution of file sizes in both PC’s and RISC workstations at USF.

![Figure 1 - Call hold times for the USF PPP modem pool used for dial-in Internet access by students](image-url)
Analysis of aggregated traffic traces at the packet level is not sufficient for developing accurate traffic models, instead the behavior of the traffic sources needs to be studied and source-destination correlations in packet streams need to be characterized. That is, the behavior of network users, applications (including their data objects), and underlying protocol implementations need to be characterized. In addition, if traffic sources can be described in algorithmic terms and not only as probability distributions, then very accurate models for simulation of individual traffic sources can be implemented. Very recent work in traffic modeling has begun to focus on the behavior of users, applications, and protocols. For example, in [73] self-similarity is explained in terms of the Noah and Joseph effects suggesting that user behavior may be at the root of these effects. In [58] the observation of very few very large FTP transfers is made. In [56] the objects (files) in a file system are studied with the goal of better understanding of network traffic. Recent work has also begun to study source-destination correlations in traffic traces and the effects of these correlations on increasing delay in ATM switches (see, for example, [76]).

Simulation studies can use probability distributions and trace-driven inputs as traffic models. In addition, in some cases, subsets of actual protocol implementations can be built-in to the simulation model (see, for example, the simulation of TCP/IP Vegas using the Xkernal in [5] and TCP/IP Reno using the ns simulator in [56]). The use of tractable probability distributions for traffic models is required in analytical models, but may be overly restrictive (and inaccurate) for simulation modeling. Trace driven traffic models are necessarily limited in scope and not well suited for future applications. The tcplib workload library simulation in [22] and the SURGE WWW workload generator in [3] represent algorithmic approaches to traffic models based on characterizations of user behaviors (e.g., distribution of telnet connection interarrival times in tcplib). In [59] network traffic is expressed as a hierarchy of generative behaviors. A generative model based on a context free grammar is used as an input to a simulation model of a client/server system to optimally assign clients to a server. Little work has been done in developing traffic models for expected gigabit applications such as image serving and high definition video delivery. Methods of studying user, application, and protocol behaviors as a means of understanding network traffic need to be advanced and unified for gigabit networks. In addition, a better understanding of source-destination correlation properties of traffic bursts is needed for studying switch performance.

3.3 Input buffered switches, QoS scheduling in switches, Gigabit FDR, and PAUSE flow control

Switch architectures can be classified by their organization of buffers and whether their switch fabric is blocking or non-blocking. Switches with cross-bars or high-speed buses (where the bus transfer rate exceeds the sum of port data rates) are non-blocking. A non-blocking switch with output buffering requires memory speeds equal to the sum of switch port data rates. The memory bandwidth requirement for a shared-buffer architecture is even greater. Thus, memory speeds are the bottleneck to high port densities for switches with output buffering. Given a 64-bit wide memory with a speed of 10 nanoseconds per read/write cycle, a maximum of six gigabit ports could be implemented in a switch using this memory. Input buffered only switches require memory speeds no faster than the data rate of the input port links and can thus scale to large port densities. However, simple input buffered only switches suffer from HOL blocking and in the case of input traffic, with uniformly distributed target output ports, achieve a maximum of 58% throughput (for high port count), see [35]. If the destination port of input traffic is not uniformly distributed, but is instead bursty with all the cells or packets in large bursts having the same destination port, the throughput performance of input buffered only and input and output buffered switches are close to the same, see [46]. With synchronized periodic traffic streams, stationary blocking can occur with significantly lower throughput than in the uniformly distributed case, see [40]. The significance is that with real traffic distributions, the HOL blocking problem in input buffered only switches is not fully understood and requires further study.

Since the finding in [35], significant research has been done to overcome the 58% throughput limit. The methods used to overcome HOL blocking and its 58% throughput limit include increasing the internal bus speed (see [7]), using non-FIFO readable input buffers (see [34]), and using parallel input queues (one for each output port) at each input port (see [68]). Figure 2(a) shows an input buffered switch. Figure 2(b) shows the same with parallel input queues at each of \( N \) ports. For the latter case, fast input-output matching algorithms can be developed to achieve full 100% (i.e., non-blocking) throughput for an offered load of cells with uniformly distributed destination output ports. The study of such algorithms is a difficult problem and has only been done for fixed-length cell switch architectures. In [1] the Parallel Iterated Matching (PIM) algorithm is developed. PIM implements a statistical matching of input and output ports over a number of iterations per forwarding cycle. In [47] 100% throughput with a “practical scheduling algorithm” called Iterative Round Robin Matching with Slip (iSLIP) is described and proved. The iSLIP algorithm is a non-random implementation of PIM that uses rotating arbiter counters for each port where the match criterion is to minimize the distance between the input and output ports and respective counters.
Buffers \hspace{1cm} Switch fabric and arbitration \hspace{1cm} Parallel input queues

(a) \hspace{5cm} (b)

Figure 2 - Input buffered only switch architecture with (a) single and (b) parallel input queues

Existing Weighted-Fair Queueing (WFQ) (see [23]) and Deficit Round-Robin (DRR) (see [63]) algorithms for QoS support assume output buffered switches. Their application to input buffered only switches is a non-trivial problem. In [45] the Fair Arbitrated Round Robin (FARR) scheduling algorithm is presented and evaluated for an input buffered only ATM switch. In FARR received cells are time-stamped and placed in priority queues for each port. Then, instead of iterated random matching as in PIM, matching is based on time-stamp age and priority. Similar to the statistical matching of PIM, multiple iterations are still required with FARR. Simulation results are presented for traffic models of combined voice, video, and data, and for uniform and non-uniform data traffic. The presented results show that FARR is fair and results in low delays. Results are not presented for maximum achievable throughput. Due to the need for several iterative rounds per matching cycle, 100% (i.e., non-blocking) throughput and scaling to high port densities may be difficult to achieve. The research in the area of scheduling algorithms for input buffered only ATM switches needs to be extended to variable packet length Ethernet switches and include support for QoS.

The Gigabit Ethernet Full-Duplex Repeater (FDR) is proposed in [21] and described and evaluated in [15]. The Gigabit FDR is a buffered full-duplex repeater that uses simple round-robin scheduling to share an internal 1-Gbps bandwidth between its ports. To prevent overflow of input buffers, the Gigabit FDR uses IEEE 802.3x PAUSE flow control (see [30]) in an XON/XOFF fashion. Low and high thresholds in the input buffers determine when a PAUSE frame is to be sent to the upstream host or switch controlling the flow in the gigabit link. PAUSE flow control is not selective by IEEE 802.3p priority class (see [29]). The Gigabit FDR represents a mid-point between distributed-scheduled, shared-bandwidth Ethernet (i.e., CSMA/CD Ethernet) and centralized-scheduled, fully-parallel bandwidth Ethernet (i.e., switched Ethernet). The Gigabit FDR as originally proposed in [21] forwards all received packets to all output ports, hence output buffering is required. However, if packet forwarding is filtered by destination address, then the output buffering can be removed and the Gigabit FDR is a generic input buffered only switch with switch fabric speed-up of one. For applications typified by one-to-many traffic, the Gigabit FDR can yield equivalent performance to a fully switched Gigabit Ethernet and significantly higher performance than CSMA/CD Ethernet (see [15]). Due to its simplicity and low internal bandwidth requirement, the Gigabit FDR architecture is especially promising for scaling-up Ethernet to 10-Gbps speeds. The performance of the Gigabit FDR, its use of PAUSE flow control, its scaling to higher speeds and/or full parallelism, and the addition of priority mechanisms need to be further studied.

### 3.4 Performance of half-duplex, CSMA/CD Gigabit Ethernet

The Project Authorization Request (PAR) for Gigabit Ethernet was approved in March 1996 and resulted in the IEEE 802.3z task force which specifies both full-duplex and half-duplex (CSMA/CD) operation, see [31]. CSMA/CD assumes that the transmission time of a minimum size packet must be greater than two times the network end-to-end propagation delay ($T_{pr}$). This time period is called a slot time and a minimum packet size of one slot time is needed to
detect a worst-case collision before the transmission of the packet is complete. Computation of slot time includes medium propagation and repeater delays. For a CSMA/CD Gigabit Ethernet, an infeasible network span of about 25 meters would be needed for a 64-byte minimum packet size. Thus, the IEEE 802.3z task force has approved carrier extension and packet bursting as methods to increase the span to standard 100 meter host-to-repeater.

Carrier extension (see [27]) extends the duration of a transmission, or carrier, event to a minimum of 512 bytes by transmission of non-data symbols following a packet of less than 512 bytes in length. The collision window then includes the packet and any added non-data carrier. For a 64 byte packet, 448 bytes of overhead carrier are added. Simulation results in [51] show that for a 15 host Gigabit Ethernet with 100% offered load consisting of all 64-byte packets, the maximum achievable throughput is only about 91-Mbps.

Packet packing (see [33]) was proposed as a method of increasing the throughput of small packets on Gigabit Ethernet. In packet packing a sending host with multiple packets queued for transmission can “pack” multiple back-to-back packets in one carrier event. If the total length of all queued and transmitted packets is less than 512 bytes, the carrier is extended with non-data symbols to 512 bytes. Packet packing increases 64-byte packet throughput (for 15 hosts, 100% offered load) to about 340-Mbps. A variant of packet packing is also presented in [42] as a means of increasing the transmission efficiency of CSMA/CD networks where packet transmission time is less than the channel delay (or slot time). In [42] a host delays transmission until L packets are queued to improve the efficiency of the network. Performance evaluation results, based on a p-persistent protocol, show that the value of L should be adaptively set, L = 1 for low load and L > 1 for high load.

Packet bursting, a simpler version of packet packing, was proposed in [51] and evaluated in [52]. In packet bursting a host with multiple packets queued for transmission sends the first packet with carrier extension to 512 bytes and then sends subsequent packets without extending the carrier (i.e., the first packet’s carrier extension achieves the collision window size). Table 1 summarizes simulation results for throughput (15 hosts, 100% offered load) for carrier extension, packet packing, and packet bursting. The entry labeled “trace traffic” shows simulation results using actual 10-Mbps Ethernet workstation traffic traces (from Sun Microsystems, Inc.) as input (see [27]). A key assumption to the efficiency of both packet packing and packet bursting is that a single host can queue and transmit multiple packets in a “back-to-back” fashion. It is unlikely that this assumption can be met. That is, the delay between successive packet transmissions does not exceed the standard 96 bit interpacket gap. If this assumption cannot be met given realistic application and protocol characteristics, packet packing and packet bursting will yield minimal throughput gains over simple carrier extension.

<table>
<thead>
<tr>
<th>Packet size</th>
<th>Carrier extension</th>
<th>Packet packing</th>
<th>Packet bursting</th>
</tr>
</thead>
<tbody>
<tr>
<td>64 bytes</td>
<td>90.68 Mbps</td>
<td>339.84 Mbps</td>
<td>286.78 Mbps</td>
</tr>
<tr>
<td>1500</td>
<td>853.20</td>
<td>853.20</td>
<td>853.20</td>
</tr>
<tr>
<td>Trace traffic</td>
<td>562.19</td>
<td>740.80</td>
<td>700.32</td>
</tr>
</tbody>
</table>

Table 1 - Gigabit Ethernet simulation results showing throughput (taken directly from [51])

4. Research Plan

This section describes the research plans for the three problems, 1) gigabit traffic modeling, 2) enabling QoS support in input buffered only switches including Gigabit full-duplex repeaters, and 3) efficient small packet support for half-duplex CSMA/CD operation. Development of a research and teaching laboratory is described in Section 5.4 and expected research outcomes are described in Section 6.2

4.1 Studying traffic for gigabit applications

The first step in studying gigabit traffic is to identify likely applications requiring gigabit bandwidths. Workgroup applications that can benefit from gigabit bandwidth include image serving, WWW server clustering, network caching for data-intensive computing applications, and high definition video delivery. As a backbone, gigabit networks will carry superimposed traffic from many different applications and sub-networks. This research will focus on single traffic sources (e.g., as in workgroup networks at the edge of a larger network). The key premise in this research is that network traffic can best be characterized, and ultimately modeled, by studying the behavior of the users, data objects, and application and protocol implementations. For example for image serving, request interarrival times, request sizes, image popularity, image sizes, temporal locality, and application and protocol-related packet...
transmission behaviors all need to be characterized. The first application to be studied will be medical imaging. This application is selected first for two reasons, 1) medical imaging is a key candidate for use in high-bandwidth networks, and 2) the ready availability of medical imaging systems at the University of South Florida (see [62]). The modeling procedure will be:

1. Characterize user behavior via traces collected by instrumentation of user client systems (for example, through the use of the Application Response Measurement (ARM) interface from [2]).
2. Characterize data objects via traces collected by direct study of data storage.
3. Characterize application and protocol behavior via traces collected by instrumentation of the application and protocol implementations.
4. From the collected traces, hierarchical algorithmic models will be developed that describe interarrival times of application requests, interarrival times of packets, and source-destination correlations.

The second application to be studied will be the delivery of high-definition video on gigabit networks. The characteristics of the video coding and its delivery to the network will be studied by instrumenting video sources. NASA-KSC is investigating usage of high-definition video for monitoring space shuttle launches. Contacts established at NASA-KSC during the summer of 1998 will be used to gain access to high-definition video hardware and software.

The use of software instrumentation, especially within higher-layer protocol implementations, to collect trace data associated with network traffic is believed to be an innovation unique to this research. Studying how packets are multiplexed on a link (e.g., when serving multiple overlapped image requests) is a key challenge of this research component. This will require understanding the behavior of higher-layer protocols, such as TCP/IP, and their relationships with the operating system and application implementations. The level of packet multiplexing will largely determine the source-destination correlation structure of traffic bursts. The developed models will be used to generate synthetic traffic traces which will be directly validated with collected network traffic traces.

The results from this research component will be accurate traffic models to use as inputs for models of Gigabit Ethernet networks and advancement of new methods for studying and modeling traffic. This leads into the next research component of this CAREER program.

4.2 Enabling QoS support in input buffered only switches and full-duplex repeaters

Studying scheduling algorithms and QoS in input buffered only switches and repeaters is a key component of this CAREER program. Four specific sub-problems will be addressed:

1. The evaluation of input buffered only switch performance given realistic traffic.
2. The definition and evaluation of a new selective PAUSE flow control based on the eight priority levels in IEEE 802.3p and of a new rate control RATE MAC frame.
3. The advancement of feasible and efficient scheduling and support for priority in input buffered only variable-length packet switches.
4. The scaling of the Gigabit FDR to internal speed-up between 1 and $N$ ($N = \text{number of ports}$) and the efficient support of priority classes via selective PAUSE from (2) and (3) above.

As a first step, performance models of input buffered only switches, input-output buffered switches, and full-duplex repeaters will be built. The models will be built using the principal investigator’s new station-centric approach of [16] and will isolate the scheduling portion of the implementation in a separate module. In the case of the Gigabit FDR, the simulation model will be validated against actual hardware (see Section 5.4) in the laboratory. Input to the models will include arrival streams following a Poisson process and with target output ports selected from a uniform distribution. With this classic traffic model, the effects of fixed-length versus variable-length packet sizes will initially be studied. The traffic models of the first research component (of Section 4.1) will be used to study the effects of real traffic on switch performance and, in particular, comparative performance of input buffered only versus input-output buffered switches. New results are expected to show that simple input buffered switches do not perform much worse than input-output buffered switches given realistic traffic input from expected gigabit applications.

The IEEE 802.3x PAUSE flow control mechanism has no specified policy for its use. PAUSE policies will be investigated in the context of input buffered only switches and full-duplex repeaters. In particular, the creation of a selective PAUSE associated with the eight levels of priority in IEEE 802.3p will be proposed and studied. The PAUSE flow control mechanism is probably inadequate for multi-hop configurations due to multiple flow fairness problems (e.g., see [53]). Fairness problems with PAUSE policies will be studied and solutions proposed and evaluated. Flow control experiments will include:
The effects of PAUSE flow control on higher-layer flow control behavior (e.g., TCP/IP slow start and congestion avoidance).

The use of probabilistically generated PAUSE values to prevent synchronization between transmitting hosts.

The extension of the standardized PAUSE mechanism to include a priority field based on IEEE 802.3p service class definitions and its use in enabling QoS support for packet flows through switches and repeaters.

The extension of the above selective PAUSE mechanism to include a specifiable host transmission rate via a new RATE MAC frame. This can minimize the number of MAC frames that need to be sent and can also be used to enforce fairness and priority rules.

This research component will create new knowledge for flow control policies for Gigabit Ethernet networks using and extending the standardized PAUSE mechanism that to date has not been studied in much depth.

It is hypothesized that bursty, best-effort data traffic and guaranteed-service traffic streams can be supported in an input buffered switch by prioritizing and controlling traffic streams before allowing them to enter the core of an input buffered switch. Figure 3 shows the proposed switch architecture with \( P \) parallel input queues per port (\( P = 8 \) for IEEE 802.3p), followed by \( N \) parallel input queues where \( P \) is the number of priority levels and \( N \) is the number of ports. Previous work (see [46]) has assumed that an infeasible \( NP \) queues are needed for each port if priority is to be supported with high throughput efficiency. This research will show that a feasible \( N + P \) queues as shown in Figure 3 can suffice. The switch core (shown with the dotted lines in Figure 3) implements an existing iSLIP, or other, scheduling algorithm to achieve very high throughput efficiency. External to the core the priority classes are managed. For each priority queue at each port, a priority round robin will be studied as a means of access to the switch core. To maintain max-min fairness between priority classes in the case of inadmissible loads, the use of both PAUSE and RATE mechanisms will be studied. In addition, packet spacing and bursting at the edge of the switch core can be used to maintain service requirements for the priority classes.

![Figure 3](image)

**Figure 3** - Input buffered switch with double parallel input queues (switch core is within the dotted lines)

Using packet spacing, the peak bandwidth usage of a priority queue can be limited to a predetermined value. Figure 4 shows a C-like pseudocode description of the algorithm implemented at each input port at the entrance to the switch core whereby a priority queue is only allowed to forward packet(s) if a calculated `packet_gap_time[i]` has expired. The `packet_gap_time[i]` is computed as the last packet transmission time divided by the percentage of total bandwidth the priority class has been allocated, subtracted by the last packet transmission time. In
the case of a time greater than \( \text{packet\_gap\_time}[i] \) before a priority queue with packet(s) queued is subsequently polled, the next port time-out period, timed by \( \text{timer}[i] \), is appropriately reduced (as shown on line 8 of Figure 4). Thus, the mean port time-out period is constrained to be equal to, or greater than, the computed mean \( \text{packet\_gap\_time}[i] \). The \( i \) is the index for priority queues at each input port. The key premise is that distributed scheduling and control within the individual switch ports, rather than a single global scheduling policy, can best achieve efficient QoS support in an input buffered only switch.

1. \( i = 0; \)
2. while(1) {
3.   if ((\text{priority\_queue}[i] has a packet queued) && (\text{timer}[i] \leq 0)) {
4.     remove a packet from \text{priority\_queue}[i];
5.     wait for equivalent of a packet transmission time;
6.     compute \text{packet\_gap\_time}[i];
7.     set \text{timer}[i] to \text{packet\_gap\_time}[i];
8.     subtract from \text{timer}[i] time since last transmission;
9.     start \text{timer}[i] if its value is greater than zero;
10. }
11. }[
12. ]

1. \( j = 0; \)
2. while(1) {
3.   if ((\text{in\_port}[j] has a packet queued) && (\text{target\_port} is idle)) {
4.     \text{xmit\_count}++;
5.     invoke transmit process for transmission at \text{target\_port};
6.   }
7.   if (\text{xmit\_count} == \( M \)) wait until \text{xmit\_count} < \( M \);
8.   }[
9. ]

**Figure 4** - Round robin polling of priority queues with packet spacing (implemented at each input port)

Improvements to the efficiency and fairness of a full-duplex repeater can be achieved by implementing scheduling algorithms based on the known state of each input queue in the repeater. The scheduling discipline must be max-min fair. An implementation of the ideal Generalized Process Sharing (GPS) that can support variable length packets is needed. The DRR and WFQ algorithms both handle variable length packets and are fair within the bounds of the largest packet length. Both the DRR and WFQ methods will be modeled for a full-duplex repeater. To scale-up the internal bandwidth of the repeater will require changing the scheduling algorithm. This type of scaling will allow the implementation of a new device between a repeater and switch (a repeater/switch) in the quantity of internal bandwidth. Parallel scheduling will be used to match input and output ports where all ports are serviced with port selection continuing until \( M \) parallel packet transmissions are in progress representing an internal bandwidth of \( M \) Gigabits per second. This scheduling will thus allow gigabit repeater/switch bandwidths to scale in one gigabit increments. Figure 5 shows a C-like pseudocode description for parallel round-robin scheduling (weighting for variable packet sizes to support WFQ or DRR is not shown). In this description, \( N \) is the number of ports, \( M \) is the number of allowed parallel transmissions (\( 1 \leq M \leq N \)), \( j \) is the index for input ports, and the transmit process (not shown) asynchronously decrements \( \text{xmit\_count} \) on completion of a packet transmission.

1. \( \text{xmit\_count} = 0; \) \( j = 0; \)
2. while(1) {
3.   if ((\text{in\_port}[j] has a packet queued) && (\text{target\_port} is idle)) {
4.     \text{xmit\_count}++;
5.     invoke transmit process for transmission at \text{target\_port};
6.   }
7.   if (\text{xmit\_count} == \( M \)) wait until \text{xmit\_count} < \( M \);
8.   }[
9. ]

**Figure 5** - Parallel round-robin scheduling as proposed for a full-duplex repeater/switch

The performance of the parallel scheduling will be evaluated, extensions and improvements will be made. The weighting of ports, or port priorities, for adjusting transmission priorities will be investigated. For example, ports used for cascading of repeaters may need to be given high priority if buffer sizes are to be kept small. Trade-offs of throughput, packet loss, and fairness will be evaluated. Both expected typical and extreme configurations and traffic loads will be evaluated. Experiment configurations will include:

9
- Small and large span Ethernets including topologies with mixed host-to-repeater propagation delays.
- Small and large population Ethernets.
- Cascading of repeaters and repeater/switches to build larger than single repeater networks.

Performance evaluation will include significant experimental work based on a full-duplex repeater and Gigabit Ethernet adapters (see Section 5.4).

Having studied QoS in full-duplex repeated and switched Ethernet networks, the final research component of this CAREER program will study and improve the performance of half-duplex Gigabit Ethernet networks.

4.3 Efficient small packet support using CSMA with Timed Collision Detection (CSMA/TCD)

To improve upon the inherent inefficiencies of carrier extension and packet bursting in half-duplex, CSMA/CD Gigabit Ethernet, CSMA with Timed Collision Detection (CMSA/TCD) will be proposed and studied. The CSMA/TCD is a new method of delayed collision detection and is intended to allow 64 byte packets to be transmitted without carrier extension on a half-duplex Gigabit Ethernet with a 512 byte slot time. It allows a sending host to detect and correctly handle a collision after a completed packet transmission. For a receiving host, the CSMA/TCD method utilizes a discard policy for packets that may have been received by some hosts, but have not been received by other hosts due to a collision. The CSMA/TCD method also has possible applications to wide-area use of Ethernet and future 10-Gigabit where any methods using carrier extension would become completely untenable. The CSMA/TCD method is described below in terms of sending host behavior, receiving host behavior, and repeater behavior.

**Sending host:** In addition to standard IEEE 802.3 MAC functions (see [6]), a CSMA/TCD sending host will perform the following functions. A sending host will maintain a transmit buffer of length 512 bytes (i.e., one slot time) which contains packets that should be retransmitted given a collision. A sending host also maintains a slot timer whose function is described below. CSMA/TCD specific functions are:

- All packets that have started their transmission within a slot time are maintained in a transmit buffer. Packets that have started their transmission in excess of one slot time are removed from the transmit buffer (i.e., are considered successfully transmitted).
- A host that has started a packet transmission within a slot time of receiving a jam signal considers itself to have collided.
- A collided host, after a normal collision backoff, retransmits all packets transmitted within the original slot time (i.e., those packets in the transmit buffer) of receiving the jam signal.

**Receiving host:** In addition to standard IEEE 802.3 MAC functions, a CSMA/TCD receiving host will perform the following functions. A receiving host will maintain a receive buffer of length 512 bytes which contains packets that should be discarded given a collision and will maintain a slot timer. CSMA/TCD specific functions are:

- All packets that have been received within a slot time are maintained in a receive buffer. Packets that have been received in excess of one slot time are passed “up” to the higher layer protocols (i.e., are considered successfully received).
- A host that has received a packet within a slot time of receiving a jam signal discards those packets from its receive buffer.

**Repeater:** In addition to standard IEEE 802.3 repeater functions, the CSMA/TCD repeater provides backwards compatibility with CSMA/CD packet bursting. Packets flowing between CSMA/TCD ports have no carrier extension added, packets flowing between CSMA/CD and CSMA/TCD ports have carrier extension added followed by bursting (CSMA/TCD-to-CSMA/CD) or have carrier extension removed (CSMA/CD-to-CSMA/TCD). Standard Ethernet autonegotiation can be used to configure a repeater port for either CSMA/CD or CSMA/TCD.

Packet bursting achieves benefits only if a host has multiple packets to send in a burst. This will not always be the case, and thus packet bursting will not achieve its theoretical efficiency improvement. The CSMA/TCD method will allow multiple hosts to each send small packets in one slot time with expected efficiency improvements for medium and large population Ethernets. However, the TCD method will likely also cause extra collisions (compared to carrier extension and packet bursting hosts) to occur in an Ethernet with high offered load. For small packets the overall behavior of a Gigabit TCD Ethernet will be very similar to that of a 1-persistent CSMA network. Thus, there exists a performance trade-off between the inefficiency of carrier extension and the lower attainable throughput of a pure CSMA network. It is expected that CSMA operation can exceed the performance of packet bursting. Significant work was completed in the 1970’s and 1980’s showing that a CSMA network with an appropriate persistence scheme can achieve very high utilization (see, for example, the classic work in [38]). If the number of collisions caused by TCD hosts is excessive (and thus degrading the overall Ethernet performance) the TCD method must be refined.
Refinements could include adaptive switching between carrier extension and TCD operation, changes to the persistence, or changes to the collision arbitration algorithm. Due to the complexity of the CSMA/TCD protocol, host behavior, and traffic models, simulation methods will be used for the performance evaluation. A station-centric approach (see [16]), which can model varying propagation delay effects, will be used. Both (expected) typical and extreme Gigabit Ethernet configurations and traffic loads will be evaluated. The correct operation of the CSMA/TCD protocol will be verified (e.g., that there are no duplicated or lost packets). Experiment configurations will include:

- Small and large span Ethernets including topologies with mixed host-to-repeater propagation delays.
- Small and large population (including multiple repeater configurations) Ethernets.
- Configurations with a mixture of CSMA/CD packet bursting and CSMA/TCD host types.

Specific experiments will be designed to investigate stability of the Ethernet, possible capture effect conditions, and fairness of interoperability given mixtures of host types.

5. Education Plan

The results from the research component of this CAREER program will provide dynamic synergism to the development of new courses and curricula, involvement and mentoring of graduate and undergraduate students in research, development of an Information Systems infrastructure including a laboratory and research tools, establishment of industry partnerships, and enhanced community service. The education plan serves as a path into the classroom for the research results. This section begins with a description of the principal investigator’s education accomplishments and ends with a discussion of education evaluation methods to be used.

5.1 Description of education accomplishments by the principal investigator

In the past three years the principal investigator has developed and taught two new graduate courses, two new undergraduate courses, and also taught two established undergraduate courses. These courses are:

- **Introduction to Computer Networks** (new graduate course)
  - An introduction to the design and evaluation of computer networks with an emphasis on analytical performance evaluation (queueing theory and traffic modeling).

- **Advanced Computer Networks** (new graduate course)
  - An advanced treatment of the single queue, networks of queues, time series analysis including long range dependence, and simulation methods. The course requires a “conference quality” project.

- **Introduction to Computer Networks** (new undergraduate course)
  - An introduction to the design and implementation of computer networks. The course covers architecture, local and wide area networks, bridging and routing, TCP/IP, and emerging high-speed technologies. This course is less analytical (and more descriptive) than the graduate course.

- **Introduction to Computer Simulation** (new undergraduate course)
  - An introduction to discrete event simulation for modeling of information systems. The course is largely based on case study examples and individual student programming projects.

- **Logic Design** (existing undergraduate course)
  - A classic first course in logic design (combinational logic through sequential machines).

- **Computer Tools for Engineers** (existing undergraduate course)
  - A required core course for all engineers that covers the use of spreadsheets, mathematics packages, and FORTRAN77 programming for solving engineering problems, see [17].

The two new undergraduate courses were rated, by required state of Florida student evaluations, as the second and third best courses in the College of Engineering for Spring 1996 (for courses with more than 15 students enrolled) and continue to be rated in the top 10% of courses in the College of Engineering. The principal investigator has made significant use of the WWW in making course materials accessible to all students. The completeness of the WWW pages is so significant that the course pages for **Introduction to Computer Networks** have been used in a Sloan Foundation funded workshop (see [64]) as one of ten examples of how to put course materials on the WWW (and has been published in [111]). Recently, an internal University of South Florida proposal has been submitted (see [12]) to develop methods for students in a freshman **Foundations of Engineering** course to learn to use the WWW as a technical communications medium by publishing draft and final project reports on the WWW.

The principal investigator has graduated four M.S. students and currently has four M.S. students and two Ph.D. students in various stages of completion. In the area of community service, the principal investigator has worked as a
volunteer with the “Yes, We Care” program (see [75]) and in judging of regional and state science fairs. “Yes, We Care” is a middle and high-school level program intended to encourage minority students to pursue science and engineering careers. The short-term goal of “Yes, We Care” is to improve the grades of the participating students. In 1997, the principal investigator was awarded an University of South Florida outstanding undergraduate teaching award for 1996/1997.

5.2 Development of courses and curricula

As part of the CAREER program, four new courses will be developed, two graduate and two undergraduate. These new courses will be part of the Information Systems degree track at the University of South Florida. As a new faculty member in this (also new) program, a unique opportunity exists to develop courses and curriculum. The courses to be developed are:

- **Performance Evaluation of Computer Networks** (graduate)
  - This will be an advanced course in performance modeling and queueing theory. Traffic models will be covered with a special emphasis on recent developments in long-range dependent models. This course will entail completion of a measurement-based modeling project. Students will measure actual network traffic and compare trace driven simulation with theoretical and simulation results based on traditional short-range traffic models. One goal in this project is for students to reproduce the results in [26]. The two text books for this course will be [36] and [37].

- **Information Systems Industry Project** (graduate - tentative with departmental curriculum decision)
  - A key part of the Masters in Information Systems degree will be a 9-month industry-assigned project. This project replaces the thesis required for the Master of Science degree. The Masters in Information Systems track is still in the planning stages, but if it comes to fruition the principal investigator intends to take the lead in establishing the requirements for the industry project. The project will entail a student completing a real world industry assignment from a Tampa Bay area firm. Industry partnerships are described in Section 5.5.

- **Capacity Planning and Performance Management** (undergraduate)
  - This course will cover the fundamentals of performance measurement, workload generation, benchmarking, and queueing theory. The course will be case-study and team-project oriented. The class will be divided into teams and a common problem be assigned to all teams. Initially, the students will have “no clue” on how to solve the problem, but as the semester progresses the necessary methods and tools will be learned. At the end of the semester, competitive team presentations will be made and the best team will “win the contract”. The goal is to get industry members to participate as judges. The contest type event is popular with students and also gives them something substantial for their resume and/or portfolio. The textbook to be used is [48].

- **Advanced Computer Networks** (undergraduate)
  - This course will cover high-speed networks including signaling, traffic classes, and switch architectures. TCP/IP internals will also be covered. This course is the next step to the **Introduction to Computer Networks** course described in the previous section. In the first half of this course the students will study the “evolution” of a multiple access network (e.g., a half-duplex Ethernet) to a switched network (e.g., a switched Ethernet and/or ATM network). In this evolution, problems are introduced in areas ranging from multiple access protocols to switch architecture and flow control. The second half of the course will focus on the next higher layer, that of TCP/IP. A programming project involving TCP/IP internals will be required. LINUX will be used as the vehicle to teach TCP/IP internals. For the TCP/IP content of this course, [74] will be the text book.

The work done in developing the two new undergraduate courses will contribute to efforts by the ACM and IEEE-CS to develop guidelines for Information Systems degree programs and ultimate accreditation of such programs (see [43] and [71]). The principal investigator is currently a member of a departmental committee to develop such recommendations to the department and college. This has included submission of an NSF CRCD proposal (see [72]) that develops a model project-based Information Systems curriculum. As part of this CAREER program, the principal investigator will expand his involvement to direct participation in the ACM and IEEE-CS committee.
5.3 Involvement and mentoring of students in research - graduate and undergraduate

Students play an important role in academic research. Students at all levels will be recruited for the research component in this CAREER program. The funding from this CAREER program will allow the principal investigator to directly fund two Ph.D. students. One student will pursue research in the area of switch scheduling algorithms and multiple access protocols, specifically problems (2) and (3) in this CAREER program. The second student will pursue research in gigabit traffic modeling of problem (1) in this CAREER program. The University of South Florida has a very active LINUX club with several very talented undergraduate students. To encourage these students to pursue graduate degrees, research funding will be sought from the NSF Research Experiences for Undergraduates program. The undergraduate students will participate in the experimental work, especially as related to data collection and analysis for problem (1) and in development of tools as described in Section 5.4.

5.4 Development of a laboratory infrastructure and research tools

A laboratory has been dedicated to the College of Engineering Information Systems program. Work is currently underway to acquire equipment and software. The CAREER program grant and matching funds from the department will enable the purchase of equipment to be used for experimental research. A testbed of six Pentium II personal workstations attached to a Gigabit Ethernet network will be built with the following components:

- One Gigabit Ethernet full-duplex repeater starter kit from Packet Engines, Inc. (see [55]). The starter kit consists of a Gigabit Ethernet full-duplex repeater and six Gigabit Ethernet PCI network interface cards.
- Six high-end Pentium II personal computers to be used for experimental work and execution of simulation models. Each workstation will include a 10/100-Mbps Ethernet adapter and a Gigabit Ethernet adapter.
- One half-duplex 100-Mbps Ethernet repeater. The 100-Mbps and 1000-Mbps Ethernet networks will be used for experimental purposes including assignments from the Advanced Computer Networks course.
- One 10/100-Mbps Ethernet switch with a Gigabit Ethernet uplink. The switch will also be used for experimental purposes. All switches will support PAUSE flow control.

Initial availability of half-duplex CSMA/CD Gigabit Ethernet is not expected. However, availability is expected in the second year of this CAREER program. Money has been budgeted in this CAREER program to “upgrade” the 100-Mbps CSMA/CD to Gigabit CSMA/CD Ethernet at that time (in addition to the full-duplex Gigabit Ethernet).

In addition to the physical infrastructure, a software infrastructure of research tools also needs to be developed. The principal researcher has created a set of simple traffic analysis tools primarily for teaching purposes and posted them on the WWW for community use (see [70]) and intends to continue in this direction. For example, these tools will be extended for use in analyzing WWW access logs. Another tool that will be developed will be a means of parallel independent execution of discrete-event simulation programs building on the work in [41]. This tool will enable network-attached computers to be used to complete simulation studies faster than could a single computer. Peer researcher and student contributions will be solicited for these research tools.

5.5 Establishment of industry partnerships and enhancement of community service

A major component of the proposed Masters in Information Systems will likely be a 9-month industry project. The industry project will entail a graduate student completing an assignment that is derived from a “real world” industrial problem. Developing industry partnerships, many within the Tampa Bay area, will be essential. The research results from this CAREER program will open doors to area companies by demonstrating the potential of the networking research at the University of South Florida to produce quality research results and graduates suitable for employment. The Tampa Bay area includes major high-technology firms with a communications and networking emphasis including GTE Data Services, IBM Global Services, and numerous smaller firms including minority-owned 8-A defense contractors. Partnerships will be sought with a range of these firms.

The principal investigator will increase his involvement with the “Yes, We Care” program (described in section 5.1) and other high-school related outreach programs. It is at the high-school level where underrepresented groups can be reached and motivated to pursue educational objectives towards mathematics, science, and engineering. The principal investigator uses a novel role playing method of teaching “Yes, We Care” high-school students basic principles of computer networks. This method can be extended to teach the fundamentals of computer operation with students acting-out roles as the processor, bus, memory, input/output units, and so on. The principal investigator intends to document this novel approach for use by others.
5.6 Evaluation of Education Activities

Mid-course formative and a final summative evaluations will be conducted following the guidelines of [67]. The formative evaluations will address implementation and progress questions including:

1. Implementation - has the project plan been followed and if not, what deviations occurred and why?
2. Implementation - have the industrial participants been identified and made actively involved?
3. Implementation - are research dependencies on schedule?
4. Progress - do the new courses provide preparation for graduate study and/or career for the students?
5. Progress - do the new courses meet the anticipated needs of the Tampa Bay area industries?
6. Progress - can the new courses be implemented in a typical curriculum?
7. Progress - which components of the new courses are effective, and which are not?

These questions will be answered via dialogue with industrial participants, surveys sent to alumni of the program, and feedback from other researchers and educators in the field.

6. Program Schedule and Expected Outcomes and Benefits

This CAREER program is planned for a duration of four years. In this section the schedule with milestones is described. Research and education outcomes and benefits are also described.

6.1 Overall schedule

The three research problems are phased across the four years of the CAREER program, the education plan is ongoing for the entire duration. Figure 6 shows the overall schedule time line with milestones.

![Figure 6 - CAREER program time line with milestones](image)

CAREER program milestones:

1. Completion of purchase of equipment listed in Section 5.4. Establishment of a WWW site to contain research results, research and teaching tools, feedback forms, and a bulletin board for community participation. It will be an ongoing background effort to maintain this site.
2. Completion of a validated image serving algorithmic traffic model based on the method described in Section 4.1. Ongoing work to build models for other gigabit applications. Publication in a major conference (e.g., IEEE GLOBECOM or IEEE INFOCOM).
3. Completion of simulation models for input buffered switches and associated traffic shaping and input-output matching algorithms. Use of traffic models from milestone (2).
4. Completion of performance evaluation, based on simulation and experimental methods, of new scheduling and traffic control methods for input buffered switches and full-duplex Gigabit Ethernet repeaters. Completion of a journal paper (e.g., for IEEE Journal on Selected Areas in Communication) covering problems (1) and (2) from this CAREER program.
5. Laboratory experiments with Gigabit Ethernet assuming a second year availability of half-duplex CSMA/CD Gigabit Ethernet adapters and repeaters.
(6) Completion of a performance evaluation of CSMA/TCD and packet bursting. Presentation to IEEE 802.3 of pertinent performance results. Completion of a journal paper.

(7) Workshop to further disseminate research results and assess future research directions.

(8) Introduction of new classes described in Section 5.2, a = Performance Evaluation of Computer Networks, b = Advanced Computer Networks, c = Capacity Planning and Performance Management, and d = Information Systems Project (tentative). Formative evaluations of education activities will be conducted at (8b), (8c), and (8d).

(9) Contributions to ACM and IEEE-CS Information Systems curriculum efforts, including ongoing committee participation. Completion of a summative evaluation of education activities.

The workshop of milestone (7) will be held in conjunction with a major networking conference. Through the workshop, new ideas will be generated for all participants to take back to their own programs.

6.2 Research outcomes and benefits

The expected research outcomes from this CAREER program include significant contributions to the rapidly growing area of Gigabit Ethernet networks. Key contributions include:

- Advancement of traffic modeling methods to extend to the understanding of user, application, data object, and protocol effects on network traffic.
- Advancements in architectures for high-throughput, scalable, and QoS-supporting packet switches.
- Contributions to IEEE 802.3 for selective PAUSE flow control by IEEE 802.3p priority levels and a RATE control MAC frame.
- Contributions to IEEE 802.3 for backwards compatible methods for efficient support of small packets on large span, half-duplex Ethernets.
- Generally available (e.g., via the WWW) traffic models for Gigabit Ethernet applications.
- Generally available simulation models for Gigabit Ethernet switches and repeaters.
- Generally available research tools for improved traffic and analysis, and simulation model execution.
- Development of a research infrastructure for future students and faculty in the Department of Computer Science and Engineering at the University of South Florida.

All of these outcomes will help researchers and practitioners better understand and build future high-speed networks with both ATM and Ethernet technologies. This is a benefit for a society becoming increasingly reliant on computer networks for day-to-day business, education, and government operation.

6.3 Education outcomes and benefits

The expected education outcomes from this CAREER program include significant contributions to the inclusion of a networks and performance evaluation focus in courses and curricula. The contributions include:

- A leadership role in the Information Systems program at the University of South Florida including establishment of university-industry relationships.
- Four new courses in the area of networks and performance evaluation including an industry project course.
- Development of a laboratory and tools infrastructure for hands-on education including projects.
- Encouragement for under-represented high-school students to pursue engineering and science at the college level and encouragement for undergraduate students to pursue graduate education.
- Contributions to the ongoing ACM and IEEE-CS efforts to establish an Information Systems curriculum.

Through these contributions, and especially the graduate Performance Evaluation of Computer Networks course, research results will be brought into the classroom. This is a significant outcome. All course materials will be published on the WWW making them easily accessible by faculty at other universities. Other outcomes include enhanced university-industry relationships and continued contributions to high-school programs aimed at recruiting under-represented student groups to engineering and science careers.
7. Departmental Endorsement

When our Department decided to develop a new degree track in Information Systems, we began our recruiting with the area of computer networks. Our first choice and first hire in that process was Ken Christensen. Dr. Christensen, in addition to having excellent credentials, also impressed us with his enthusiasm and his obvious potential to join in the construction of the new curriculum. We couldn’t have made a better choice. Dr. Christensen quickly established a research lab, attracted some excellent students and started them on projects, and joined into ongoing research activities in other labs within the Department. He also made immediate contributions to the development of our new curriculum with new course creation and existing course redesign efforts. It was most pleasing to see the fruits of our recruitment investment pay such immediate and substantial dividends.

In this proposal Dr. Christensen has outlined a most ambitious research plan. I expect him to be successful, not so much because of my evaluation of the merit of his ideas (which sound exciting but which in technical details are outside of my areas of expertise), but rather because 1) he has a demonstrated ability to do quality work within this domain, 2) he continues to attract some of our best students to work with him on research problems, and 3) he will have the enthusiastic support not only of his colleagues within our Department, but also from the communications group in the EE Department. An additional factor which will support not only this work, but also Dr. Christensen’s future research endeavors, is the presence in our metropolitan area of several companies which employ extensive and sophisticated computer networks. Their local support will be of considerable long-term importance.

We view networking to be at the core of our new Information Systems program. Dr. Christensen has already contributed new graduate and undergraduate networks courses and has developed a new simulation course. These courses are not only technically sound, but also are particularly exciting because of Dr. Christensen’s innovative inclusion of interactive, WEB-based tutorial and self-paced exercise materials. Dr. Christensen is clearly committed to bringing the best of current research and thinking to his classes. It is important to note that Dr. Christensen brings not only effort but considerable skill to his classes. As testimony to this, last year he received an Outstanding Undergraduate Teaching award from the College of Engineering. This highly competitive award had never before been given to someone in only his second year of teaching!

Our Department views Dr. Christensen as one of our most promising new faculty members. The three new faculty members which we hired two years earlier all received NSF Career Awards. Dr. Christensen is clearly following in these most challenging footsteps. We are committed to supporting his continued progress in whatever way possible. In addition to obvious support such as a research lab and supporting computer infrastructure, we will be pleased to provide an additional $10,000 of funds for specialized equipment as well as offering a release from 25% of his assigned duties for the first two years of the grant period and assuming responsibility for the tuition of Dr. Christensen’s graduate research assistants. Should other needs arise, we will make our most sincere efforts to assure that Dr. Christensen’s professional career develops to its fullest potential.

The effective date of the first full-time tenure-track appointment of Dr. Kenneth J. Christensen was August 8, 1995 at the University of South Florida. I have read and endorse this Career Development Plan.

Dr. Dewey Rundus
Associate Chair
Department of Computer Science and Engineering
University of South Florida

Date
REFERENCES CITED


[63] J. Frechtling, editor, NSF 93-152


BIOGRAPHICAL SKETCH

Kenneth J. Christensen

Assistant Professor
Department of Computer Science and Engineering
4202 East Fowler Avenue, ENB 118
University of South Florida
Tampa, Florida 33620
Phone: (813) 974-4761
Email: christen@csee.usf.edu
WWW: http://www.csee.usf.edu/~christen

Current Position (August 1995 appointment to Assistant Professor)

Assistant Professor in the Department of Computer Science and Engineering at the University of South Florida. Research interests are in performance evaluation of computer networks with an emphasis on Gigabit Ethernet networks. Teaching four courses per year including, Introduction to Computer Networks (graduate), Computer Networks Research Seminar (graduate), Introduction to Computer Networks (undergraduate), Introduction to Computer Simulation (undergraduate), Computer Tools for Engineers (undergraduate), and Logic Design (undergraduate).

Education

December 1991 Doctor of Philosophy in Electrical and Computer Engineering
North Carolina State University, Raleigh

May 1983 Master of Science in Electrical Engineering
North Carolina State University, Raleigh

December 1981 Bachelor of Science with Honors in Electrical Engineering
University of Florida, Gainesville

Combined Industry and Academic Experience

1991 - 1995 IBM Corporation, Research Triangle Park
Team leader for advanced development of future LAN and WAN directions and products.

1993 - 1994 Campbell University, Buies Creek
Adjunct faculty in the Department of Mathematics

1989 - 1991 North Carolina State University, Raleigh
Leave of absence from IBM Corporation (completion of Ph.D.)

1984 - 1985 North Carolina State University, Raleigh
Adjunct faculty in the Department of Electrical Engineering.

1983 - 1989 IBM Corporation, Research Triangle Park
Team leader for Token Ring LAN test development.
Publications Directly Related to this Proposal


K. Christensen, M. Molle, and B. Yeger, “The Design of a Station-Centric Network Model for Evaluating Changes to the IEEE 802.3 Ethernet Standard,” in second review cycle for Simulation.


Other Publications


Patents

Nine USA patents (5764634, 5680397, 5644577, 5625621, 5617419, 5561666, 5555377, 5491687, and 5349583).

Names of Collaborators

None (other than those listed on above publications).

Names of Graduate Advisors

Arne Nilsson (chair), Ioannis Viniotis, Harry Perros, and Wuschow Chou (all at North Carolina State University).

Names of Graduate Advisees

Jack Drobisz, Hiroshi Fujinoki, Franklin Gulledge, Nandini Javagal, Sifang Li, Yantian Lu, Anmol Mishra, Jesus Pinto, Rich Rauscher, and Randall Thompson (all are present or graduated M.S. or Ph.D. students at the University of South Florida).