

Design of Reversible Latches Optimized for Quantum Cost, Delay and Garbage Outputs

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Abstract

Reversible logic has extensive applications in emerging nanotechnologies, such as quantum computing, optical computing, ultra low power VLSI and quantum dot cellular automata. In the existing literature, designs of reversible sequential circuits are presented that are optimized for the number of reversible gates and the garbage outputs. The optimization of the number of reversible gates is not sufficient since each reversible gate is of different computational complexity, and thus will have a different quantum cost and delay. While the computational complexity of a reversible gate can be measured by its quantum cost, the delay of a reversible gate is another parameter that can be optimized during the design of a reversible sequential circuit. In this work, we present novel designs of reversible latches that are optimized in terms of quantum cost, delay and the garbage outputs. The optimized designs of reversible latches presented in this work are the D Latch, JK latch, T latch and SR latch.

1 Introduction

Reversible computation can be performed through circuits that do not lose information and are reversible in nature. Reversible circuits are designed using reversible gates which are logic gates that can generate a unique output vector for each given input vector, and vice-versa, that is, there is a one-to-one mapping between the input and the output vectors. There are a number of existing reversible gates such as the Fredkin gate, the Toffoli gate, the Peres gate and the Feynman gate [5, 21, 13]. Landauer has shown that for irreversible logic computations, each bit of information lost generates $kT \ln 2$ joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which the computation is performed [8]. Bennett showed that $kT \ln 2$ energy dissipation would not occur if a computation is car-

ried out in a reversible way [2]. Reversible logic has extensive applications in several emergent fields such as quantum computing, quantum dot cellular automata, optical computing, low power VLSI design etc. As pointed out in the literature, the reversible circuits are characterized by no information loss and negligible energy loss and are expected in demand for low power VLSI circuits [4]. Another promising application of reversible logic is in quantum computers as quantum networks must be built from reversible logical components [12, 22].

The important cost metrics in reversible logic circuits are the quantum cost, delay and the number of garbage outputs. Garbage outputs are the unutilized outputs in reversible circuits which exist just to maintain reversibility but do not perform any useful operations. In the existing research on the design of reversible sequential circuits, the number of reversible gates is used as a major metric of optimization [18, 15, 16, 19, 3]. The number of reversible gates is not a good metric of optimization as reversible gates are of different computational complexity, hence are of different quantum cost [10]. Recently, the design of reversible sequential circuits has also attracted the attention of researchers such as the work in [18, 3, 16, 17]. *From the survey of the existing works on reversible sequential circuits, it can be concluded that they have considered the optimization of number of reversible gates and garbage outputs, while ignoring the important parameters of quantum cost and delay.* In this work, our goal is to optimize the design of reversible sequential circuits in all the three important parameters, viz., the quantum cost (QC), delay and the garbage outputs (GOs). In this work, we have also introduced the delay of a reversible gate as another important parameter while designing an optimized reversible sequential circuit. We are introducing novel designs of reversible sequential circuits which minimize the quantum cost, delay and the number of garbage outputs compared to the existing designs in literature. The sequential circuits considered in this work are latches, such as D latch, T latch, JK latch and SR latch.

The paper is organized as follows: Section II presents the

basic reversible gates and their quantum implementation; Section III presents the delay computation in reversible logic circuits; Section IV presents the design of reversible latches. Section V provides the conclusions.

2 Basic Reversible Gates

There are a number of existing 3x3 reversible gates such as the Fredkin gate, the Toffoli gate, the Peres gate and the Feynman gate. Each reversible gate has a cost associated with it called the quantum cost. The quantum cost of a reversible gate is the number of 1x1 and 2x2 reversible gates or quantum logic gates required in designing it. The quantum cost of all reversible 1x1 and 2x2 gates is taken as unity [6, 10]. Any reversible gate can be realized by using 1x1 NOT gate, and 2x2 reversible gates such as the Controlled-V and the Controlled-V⁺ and the Feynman gate which is also known as Controlled NOT gate (CNOT). Thus in simple terms, the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V⁺ and CNOT gates used in implementing it except in few cases as shown in [6].

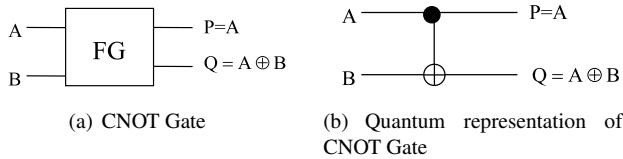


Figure 1. CNOT gate and its quantum representation

2.1 Feynman Gate (CNOT Gate)

Feynman gate (FG) or Controlled-NOT gate(CNOT) is a 2 inputs 2 outputs reversible gate having the mapping (A, B) to (P=A, Q=A ⊕ B) where A, B are the inputs and P, Q are the outputs, respectively. Since it is a 2x2 gate, it has a quantum cost of 1. Figures 1(a) and 1(b) show the block diagram and quantum representation of the Feynman gate, respectively.

2.2 Toffoli Gate

Toffoli Gate (TG) is a 3x3 two-through reversible gate as shown in Fig. 2(a). Two-through means two of its outputs are the same as inputs with the mapping (A, B, C) to (P=A, Q=B, R=A · B ⊕ C), where A, B, C are inputs and P, Q, R are outputs, respectively. Toffoli gate is one of the most popular reversible gates and has quantum cost of 5 as shown

in Fig.2(b). The quantum cost of Toffoli gate is 5 as it needs 2 Controlled-V gates, 1 Controlled-V⁺ gate and 2 CNOT gates to implement it.

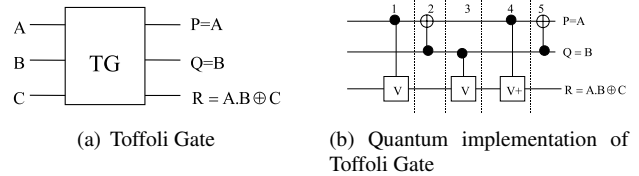


Figure 2. Toffoli Gate and its quantum implementation

2.3 Peres Gate

Peres gate is a 3 inputs 3 outputs (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q=A ⊕ B, R=(A · B) ⊕ C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. Figure 3(a) shows the Peres gate and Fig. 3(b) shows the quantum implementation of the Peres gate (PG) with quantum cost of 4 [6]. The quantum cost of Peres gate is 4 since it requires 2 Controlled-V⁺ gates, 1 Controlled-V gate and 1 CNOT gate in its design. In the existing literature, among the 3*3 reversible gate, Peres gate has the minimum quantum cost.

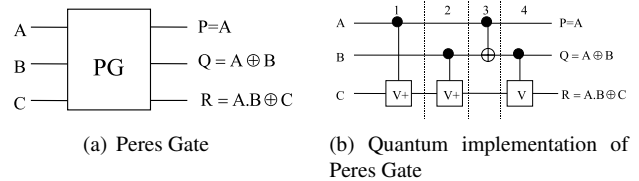


Figure 3. Peres Gate and its quantum implementation

2.4 Fredkin Gate

Fredkin gate is a (3x3) conservative reversible gate, having the mapping (A, B, C) to (P=A, Q=A' · B + AC, R=AB + A' · C), where A, B, C are the inputs and P, Q, R are the outputs, respectively [5]. It is called a 3x3 gate because it has three inputs and three outputs. Figure 4(a) shows the Fredkin gate and Figure 4(b) shows its quantum implementation with quantum cost of 5 [6]. Please note that each dotted rectangles in Fig. 4(b) is equivalent to a 2x2 Feynman gate and so the quantum cost of each dotted rectangle

is 1 [6]. Hence Fredkin gate cost consists of 2 dotted rectangles, 1 Controlled-V gate and 2 CNOT gates resulting in its quantum cost as 5.

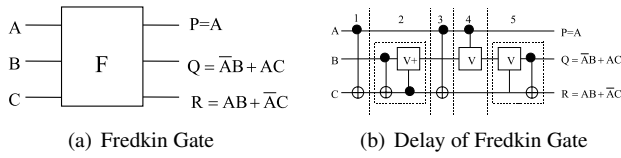


Figure 4. Fredkin Gate and its quantum implementation

3 Delay Computation in Reversible Logic Circuits

In this work, we are introducing another parameter regarding the efficiency of reversible sequential circuits which is the critical delay of the circuit. In many of the earlier works in the reversible combinational circuits such as [7, 1], delay of each reversible gate such as 2x2, 3x3 and 4x4 reversible gates, all are considered to be of unit delay irrespective of their computational complexity. This is not fair for comparison as delay will vary according to the complexity of a reversible gate. In our delay calculation we are using the logical depth as the measure of the delay [11]. The delay of all 1x1 gate and 2x2 reversible gate is taken as unit delay called Δ . Any 3x3 reversible gate can be designed from 1x1 reversible gates and 2x2 reversible gates, such as the CNOT gate, the Controlled-V and the Controlled- V^+ gates. Thus the delay of a 3x3 reversible gate can be computed by calculating its logical depth when it is designed from smaller 1x1 and 2x2 reversible gates.

The Toffoli gate, the Peres gate and the Fredkin gate are the three major 3x3 reversible gates used in this work for designing the reversible sequential latches, thus in this section we are also calculating their delays. Figure 2(b) shows the logic depth in the quantum implementation of Toffoli gate. Thus, it can be seen that the Toffoli gate has the delay of 5 Δ . Each 2x2 reversible gate in the logic depth contributes to 1 Δ delay. Similarly, the Peres gate and the Fredkin gate shown in Fig. 3(b) and Fig. 4(b) have the logic depth of 4 and 5, respectively, that results in their delay as 4 Δ and 5 Δ .

4 Design of Reversible Latches

In this section, we present novel design of reversible latches that are being optimized in parameters of quantum cost, delay and the number of garbage outputs.

4.1 SR Latch

The SR latch can be designed by using two cross-coupled NOR gates or two cross-couple NAND gates. In the existing literature, the cross coupled NOR gate strategy was used to design the Fredkin gate based SR latch and the cross-coupled NAND gate strategy was used for designing Toffoli gate based SR latch [14, 16]. The Toffoli gate and the Fredkin gate based SR latches require two Toffoli gates and two Fredkin gates, respectively, and hence will have a quantum cost of 10 and delay of 10 Δ . All these reversible SR latch designs do not have enable signal(clock), hence are not gated in nature. In this work, we first propose SR latch design without any enable signal. The design takes two Peres gate and is based on cross-couple NAND strategy. The proposed design is shown in Fig. 5(a). Since Peres gate has quantum cost of 4 and delay of 4 Δ , thus, the proposed design will have the propagation delay of 8 Δ and quantum cost of 8. The proposed design achieves an improvement of 20% both in terms of quantum cost and delay without increasing the garbage outputs as compared to the design presented in [16]. The results are summarized in Table 1.a. Further, the reversible design of gated SR latch in which the enable signal(E) controls the signal propagation is shown in Fig. 5(b). The design is constructed by replacing each NAND gate in conventional irreversible SR latch by a Peres gate. Thus the proposed design of reversible gated SR latch has the quantum cost of 16, delay of 12 Δ and needs 5 garbage outputs. In the existing literature, the gated SR latch is proposed in [18]. In [18], the gated SR latch was designed using the New gate [7], the Fredkin and the Feynman gates. The quantum implementation of the New gate was proposed in [1] and has the quantum cost of 11. The New gate has the logical depth of 11 resulting in its propagation delay as 11 Δ . The comparison of the proposed design with the design proposed in [18] is shown in Table 1.b. The proposed design achieves 52.9 %, 58.6 % and 16.66 % improvement compared to the design presented in [18], in terms of the quantum cost, delay and the garbage outputs.

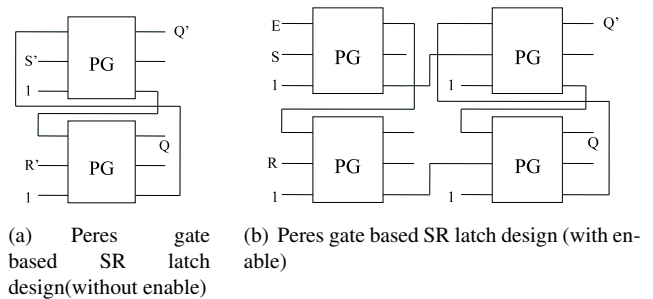


Figure 5. Peres Gate based SR latch

Table 1. A Comparison of Reversible SR Latches

(a). Reversible SR Latches without enable			
	QC	Delay	GOs
Fredkin gate based [16]	10	10	2
Toffoli Gate based [16]	10	10	2
Proposed Peres gate based	8	8	2
Improvement in % w.r.t [16]	20	20	-

(b). Gated Reversible SR Latches			
	QC	Delay	GOs
[18]	34	29	6
Proposed Peres gate based	16	12	5
Improvement in % w.r.t [18]	52.9	58.6	16.66

4.2 D Latch

The characteristic equation of the D latch can be written as $Q^+ = D \cdot E + \bar{E} \cdot Q$. It can be mapped to the Fredkin gate (F). Figure 6(a) shows the realization of the reversible D latch using the Fredkin gate and one Feynman gate (fan-out is not allowed in reversible logic) [20, 19, 3]. In this work, we calculated the quantum cost of the design shown in [20, 19, 3], its quantum cost is 6 and is realized with two garbage outputs. We observed that it cannot be further optimized in terms of the quantum cost and the garbage outputs. *The propagation delay of the Fredkin gate based D latch are also shown for the first time in literature.* Since in this design we have 1 Fredkin gate and 1 Feynman gate in series, its propagation delay is 6Δ which is the summation of 5Δ propagation delay of Fredkin gate and 1Δ propagation delay of Feynman gate. The design shown in Fig. 6(a) does not produce the complement output Q' which is required in a number of places in the sequential circuits [16]. Out of all the existing designs, only the design presented in [18, 19] have both the outputs Q and its complement Q' . The design in [18] is designed with 4 New gates and 3 Feynman gates, and thus has the quantum cost of 47. The propagation delay of the D latch design in [18] is 25Δ from input D to output Q' , and the design has 6 garbage outputs. In [19], two Fredkin gates are used in designing the D latch having outputs Q and Q' . As we know that each Fredkin gate has the quantum cost of 5, so the design presented in [19] has the quantum cost of 10 and needs two garbage outputs. Further, the design in [19] has two Fredkin gates connected in series, thus its propagation delay is 10Δ . In this work, we are proposing a novel design of D latch that has both the outputs Q and Q' and is designed with 1 Fredkin gate and 2 Feynman gates as shown in Fig 6(b). The proposed design has the quantum cost of 7 (quantum cost of 1 Fredkin gate+ quantum cost of 2 Feynman gates) and has bare minimum of two garbage outputs. The propagation delay of this design is 7Δ . A comparison of the proposed design with the existing designs is shown in Table 2 which shows that the proposed design achieves improvement ratios of 85%, 72% and 67 % in terms of the quantum cost, delay and the garbage outputs compared to the design presented in [18]. The improvement ratios compared to [19] are 30% both in terms of the quantum cost and the propagation delay, while

maintaining the minimum 2 garbage outputs.

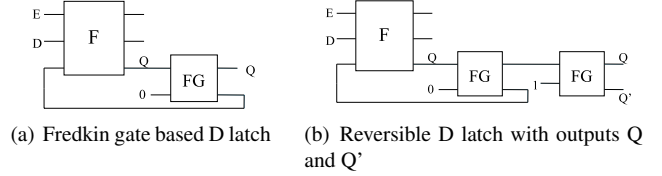


Figure 6. Designs of reversible D latch

Table 2. A Comparison of Reversible D Latches with Output Q and Q'

	QC	Delay	GOs
[18]	47	25	6
[19]	10	10	2
Proposed Design	7	7	2
Improvement in % w.r.t [18]	85	72	67
Improvement in % w.r.t [19]	30	30	-

4.3 T Latch

The characteristic equation of the T latch can be written as $Q^+ = (T \cdot Q) \cdot E + \bar{E} \cdot Q$. But the same result can also be obtained from $Q^+ = (T \cdot E) \oplus Q$. This equation can be directly mapped to the Peres gate. The fan-out at output Q can be avoided by cascading the Feynman gate. The proposed design is shown in Fig 7(a). The design has the quantum cost of 5 (quantum cost of Peres gate+ quantum cost of Feynman gate), delay of 5Δ and requires 2 garbage outputs. The existing design in literature [3], has the quantum cost of 6, delay of 6Δ and also requires 2 garbage outputs. Thus, the proposed design is better than the design presented in [3], and achieves the improvement ratios of 17% both in terms of quantum cost and delay as shown in Table 3.a. But these designs do not produce the complementary output Q' . In the existing literature, the reversible T latch design having both Q and complementary output Q' is presented in [18, 19]. In this work, we propose a novel design of T latch based on the Peres and the Feynman gates

that has both the outputs Q and Q' . The proposed design is shown in Fig 7(b) and has the quantum cost of 6, delay of 6Δ and produces 2 garbage outputs. The existing design presented in [18] has the quantum cost of 46, delay of 35Δ and 12 garbage outputs, while the design proposed in [19] has the quantum cost of 10, delay of 10Δ and 2 garbage outputs. Thus, the proposed reversible T latch with outputs Q and Q' achieves an improvement ratios of 87 %, 83% and 83% in terms of quantum cost, delay and the garbage outputs, respectively, compared to the designed presented in [18], while the improvement compared to the design presented in [19] is 40% both in terms of the quantum cost and the delay while maintaining the 2 garbage outputs. The comparison is summarized in Table 3.b.

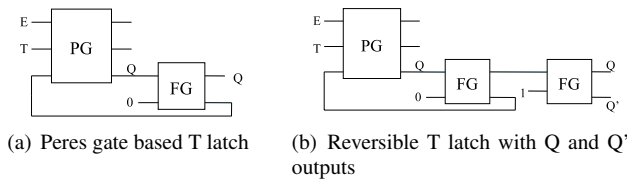


Figure 7. Designs of reversible T latch

4.4 JK Latch

The characteristic equation of the JK latch can be written as $Q^+ = (J \cdot \bar{Q} + \bar{K} \cdot Q) \cdot E + \bar{E} \cdot Q$. The equation $J \cdot \bar{Q} + \bar{K} \cdot Q$ can be mapped to the Fredkin gate as shown in 8(a) in which the input K is passed to the Fredkin gate in complement form. Thus at the second output of the Fredkin gate we will get $J \cdot \bar{Q} + \bar{K} \cdot Q$. This $J \cdot \bar{Q} + \bar{K} \cdot Q$ output can be used as an input D to the reversible D latch shown earlier in Fig. 6(a). Thus we have the complete reversible design of JK latch as shown in Fig. 8(b). The proposed design has the quantum cost of 12, delay of 12Δ and produces 3 garbage outputs. The existing design in literature [3], is designed with 2 4×4 Toffoli gates, 1 3×3 Toffoli gate and 1 Feynman gate. The quantum cost of 4×4 Toffoli gate is 13 [9], and since quantum cost is also the measure of logical depth the delay of 4×4 Toffoli gate is 13Δ . Thus the JK latch proposed in [3] has the quantum cost of 32, delay of 32Δ and needs 3 garbage outputs. Thus the design of JK Latch proposed in this work achieves an improvement of 62.5% both in terms of quantum cost and delay, while maintaining the 3 garbage outputs. The result is summarized in Table 4.a. The above discussed designs of JK latch do not produce the complement output Q' , thus we are showing another design of the JK latch in Fig. 8(c) which produces both the outputs, viz., Q and its complement Q' . The design has the quantum cost of 13, delay of 13Δ and 3 garbage outputs. The existing design in literature [18] has the quantum cost

of 46, delay of 35Δ and produces 8 garbage outputs, while another design in literature [19] has the quantum cost of 16, delay of 16Δ and produces 3 garbage outputs. Thus, the proposed design achieves an improvement of 72%, 63% and 75% in terms of the quantum cost, delay and the garbage outputs, respectively, compared to the design presented in [18]. The improvement compared to [19] is 19% both in terms of the quantum cost and the delay without any increase in the garbage outputs. The comparison is summarized in Table 4.b.

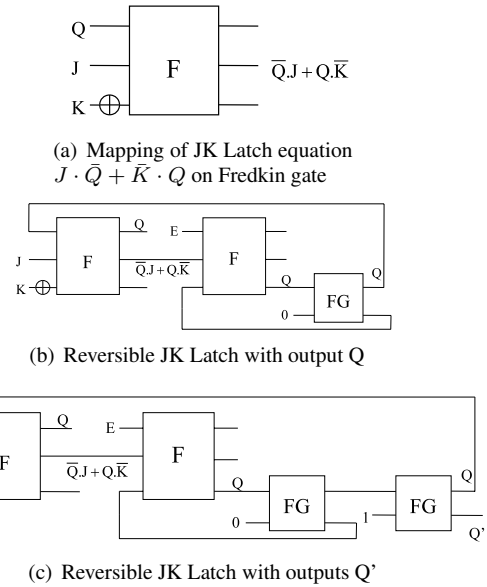


Figure 8. Designs of reversible JK Latch

5 Conclusions

In this work, we have presented novel designs of reversible latches which are optimized in terms of quantum cost, delay and garbage outputs. We conclude that the choice of reversible gates and the design approach to carefully select a reversible gate for implementing a particular logic function will significantly impact the quantum cost, delay and garbage outputs of the reversible design. As compared to the best reported designs in literature, the proposed reversible sequential latches are better in terms of quantum cost, delay and garbage outputs. Further advancement of the proposed work is to use the proposed latches towards the designs of complex reversible sequential circuits such as flip-flops, counters, storage registers and shift registers, etc. The designs of reversible sequential circuits that have asynchronous set/reset capability also need to be addressed.

Table 3. A Comparison of Reversible T Latches

(a). Reversible T Latches without Output Q				(b). Reversible T Latches With Output Q and Q'			
	QC	Delay	GOs		QC	Delay	GOs
[3]	6	6	2	[18]	46	35	12
Proposed Design	5	5	2	[19]	10	10	2
Improvement in %	17	17	-	Proposed Design	6	6	2
				Improvement in % w.r.t [18]	87	83	83
				Improvement in % w.r.t [19]	40	40	-

Table 4. A Comparison of Reversible JK Latches

(a). Reversible JK Latches with Output Q				(b). Reversible JK Latches With Output Q and Q'			
	QC	Delay	GOs		QC	Delay	GOs
[3]	32	32	3	[18]	46	35	12
Proposed Design	12	12	3	[19]	16	16	3
Improvement in %	62.5	62.5	-	Proposed Design	13	13	3
				Improvement in % w.r.t [18]	72	63	75
				Improvement in % w.r.t [19]	19	19	-

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