

A New Design of The Reversible Subtractor Circuit

Himanshu Thapliyal and Nagarajan Ranganathan
Department of Computer Science and Engineering
University of South Florida, Tampa, FL, USA
Email: {hthapliy,ranganat}@cse.usf.edu

Abstract—In [1] we have presented the reversible subtractor designs based on a new reversible TR gate (TR refers to Thapliyal Ranganathan). In [1] as the quantum gates implementation of the TR gate was not known, only the upper bound on the quantum cost of the reversible subtractors units were established. In this work, we present a new design of the reversible half subtractor based on the quantum gates implementation of the reversible TR gate. The reversible TR gate is designed from 2x2 quantum gates such as CNOT and Controlled-V and Controlled- V^+ gates. The design of the proposed reversible half subtractor is shown to be better than the design presented in [2], [1] in terms of the quantum cost and delay while maintaining the minimum number of garbage outputs. Further, we present a new design of the reversible full subtractor based on the proposed quantum gates implementation of the TR gate. The proposed reversible full subtractor is optimized in terms of quantum cost, delay and garbage outputs by utilizing the identity property of V and V^+ reversible gates. The proposed reversible full subtractor is shown to be better than the existing design reported in [3], [1]. The reversible subtractors proposed in this work will be useful in a number of digital signal processing applications.

I. INTRODUCTION

Reversible logic is emerging as a promising computing paradigm with applications in emerging technologies such as quantum computing, quantum dot cellular automata, optical computing, etc. Reversible circuits are those circuits that do not lose information and reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between the input and output vectors. Further, Landauer has shown that for irreversible logic computations, each bit of information lost generates $kT \ln 2$ joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which the computation is performed [4]. Bennett showed that $kT \ln 2$ energy dissipation would not occur if a computation is carried out in a reversible way [5]. One of the major applications of reversible logic lies in quantum computing. A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; each gate performing an elementary unitary operation on one, two or more two-state quantum systems called qubits. Each qubit represents an elementary unit of information; corresponding to the classical bit values 0 and 1. Any unitary operation is reversible and hence quantum networks must be built from reversible logical components[6], [7].

The important cost metrics in the design and synthesis of reversible logic circuits are the quantum cost, delay and the number of garbage outputs [8], [9]. The garbage outputs are the unutilized outputs in reversible circuits which exist just to maintain reversibility but do not perform any useful operations. Hence, the primary goal in reversible logic design and synthesis is to minimize the quantum cost, delay and the garbage outputs. Arithmetic units such as adders, subtractors, multipliers form the essential component of a computing system. Researchers have addressed the design of reversible adders, multipliers, comparators, sequential circuits such as in [10], [11], [12], [13], [14], [15], [16], [17]. However, the design of quantum/reversible binary subtractors has not been adequately referenced in the literature. The quantum half subtractor designed in [2] is the most popular design that is widely referenced in the literature [18], [19]. Similarly, the design of quantum full subtractor is addressed in [3]. In [1], we proposed a new reversible gate called the TR gate (TR refers to Thapliyal Ranganathan) that can singly map half subtractor output functions. We used TR gate to design the binary subtractors such as half subtractor, full subtractor and parallel subtractor. The cost of the designs were also estimated in terms of number of reversible gates, garbage outputs and quantum cost. In [1], as the quantum gates realization of the TR gate was not known only the upper bound on the quantum cost of the reversible subtractors units were estimated.

In this work, we present a new design of the reversible half subtractor based on the quantum gates implementation of the reversible TR gate. The reversible TR gate is designed from 2x2 quantum gates such as CNOT and Controlled-V and Controlled- V^+ gates. The design of the proposed reversible half subtractor is shown to be better than the design presented in [2], [1] in terms of the quantum cost and delay while maintaining the minimum number of garbage outputs. Further, we present a new design of the reversible full subtractor based on the proposed quantum gates implementation of the TR gate. The proposed reversible full subtractor is optimized in terms of quantum cost, delay and garbage outputs by utilizing the identity property of V and V^+ reversible gates. The proposed full subtractor is shown to be better than the existing design reported in [3], [1]. The reversible subtractors proposed in this work will be useful in a number of digital signal processing applications based on reversible computing where dedicated subtractor units are required.

The paper is organized as follows: Section II presents the basic reversible gates and their quantum implementation; Section III presents the delay computation in reversible logic circuits; Section IV presents the proposed reversible half subtractor; In Section V, the design of reversible full subtractor is proposed. Section VI provides the discussions and conclusions.

II. BASIC REVERSIBLE GATES

Several 3x3 reversible gates such as the Fredkin gate [20], the Toffoli gate [21] and the Peres gate [22] have been reported in the literature. The reversible gate has a cost associated with it called the quantum cost [23]. The quantum cost of a reversible gate is the number of 1x1 and 2x2 reversible gates or quantum logic gates required in its design. The quantum costs of all reversible 1x1 and 2x2 gates are taken as unity [23], [24], [25]. Any reversible gate can be realized using 1x1 NOT gate, and 2x2 reversible gates such as Controlled-V and Controlled-V⁺ (V is a square-root-of NOT gate and V⁺ is its hermitian) and the Feynman gate which is also known as the Controlled NOT gate (CNOT). Thus, in simple terms, the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V⁺ and CNOT gates required in its implementation. A few cases as exceptions are pointed out in [24].

A. The NOT Gate

A NOT gate is a 1x1 gate represented as shown in Fig. 1(a). Since it is a 1x1 gate, its quantum cost is unity.

B. The Controlled-V and Controlled-V⁺ Gates

The controlled-V gate is shown in Fig. 1(b). In the controlled-V gate, when the control signal A=0 then the qubit B will pass through the controlled part unchanged, i.e., we will have Q=B. When A=1 then the unitary operation $V = \frac{i+1}{2} \begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}$ is applied to the input B, i.e., Q=V(B). The controlled-V⁺ gate is shown in Fig. 1(c). In the controlled-V⁺ gate when the control signal A =0 then the qubit B will pass through the controlled part unchanged, i.e., we will have Q=B. When A=1 then the unitary operation $V^+ = V^{-1}$ is applied to the input B, i.e., Q=V⁺(B).

The V and V⁺ quantum gates have the following properties:

$$\begin{aligned} V \times V &= NOT \\ V \times V^+ &= V^+ \times V = I \\ V^+ \times V^+ &= NOT \end{aligned}$$

The properties above show that when two V gates are in series they will behave as a NOT gate. Similarly, two V⁺ gates in series also function as a NOT gate. A V gate in series with V⁺ gate, and vice versa, is an identity. For more details of the V and V⁺ gates, the reader is referred to [6], [24].

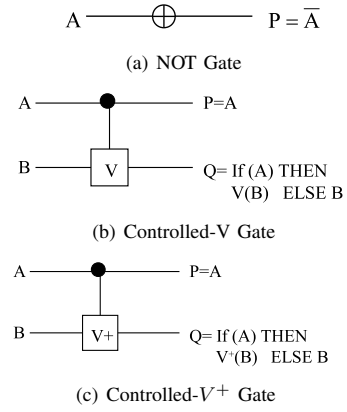


Fig. 1. The NOT and the Controlled-V and Controlled-V⁺ Gates

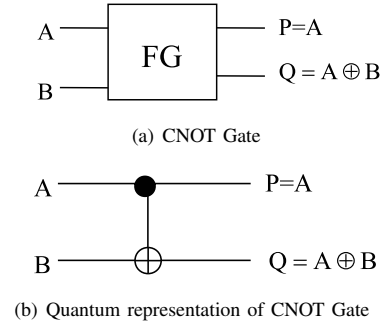


Fig. 2. The CNOT gate and its quantum representation

C. The Feynman Gate (CNOT Gate)

The Feynman gate (FG) or the Controlled-NOT gate(CNOT) is a 2-input 2-output reversible gate having the mapping (A, B) to (P=A, Q=A ⊕ B) where A, B are the inputs and P, Q are the outputs, respectively. Since it is a 2x2 gate, it has a quantum cost of 1. Figures 2(a) and 2(b) show the block diagrams and quantum representation of the Feynman gate.

D. The Toffoli Gate

The Toffoli Gate (TG) is a 3x3 two-through reversible gate as shown in Fig. 3(a). Two-through means two of its outputs are the same as the inputs with the mapping (A, B, C) to (P=A, Q=B, R=A · B ⊕ C), where A, B, C are inputs and P, Q, R are outputs, respectively. The Toffoli gate is one of the most popular reversible gates and has quantum cost of 5 as shown in Fig.3(b) [21]. The quantum cost of Toffoli gate is 5 as it needs 2V gates, 1 V⁺ gate and 2 CNOT gates to implement it.

E. The Peres Gate

The Peres gate is a 3-input 3-output (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q=A⊕B, R=(A·B)⊕C), where A, B, C are the inputs and P, Q, R are the outputs, respectively [22]. Figure 4(a) shows the Peres gate and Fig. 4(b) shows the quantum implementation of the

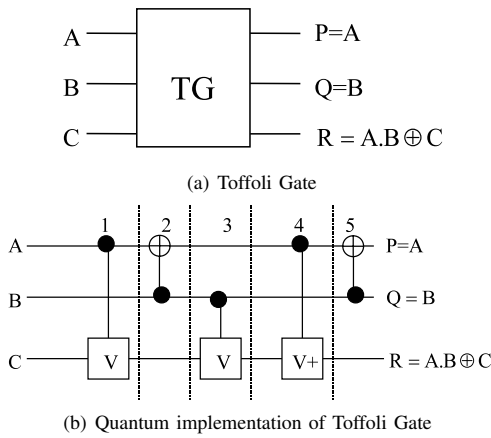


Fig. 3. The Toffoli Gate and its quantum implementation

Peres gate (PG) with quantum cost of 4 [24]. The quantum cost of Peres gate is 4 since it requires 2 V^+ gates, 1 V gate and 1 CNOT gate in its design.

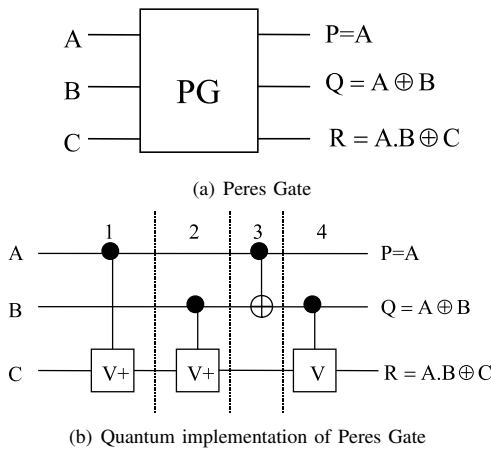


Fig. 4. The Peres Gate and its quantum implementation

III. DELAY COMPUTATION IN REVERSIBLE LOGIC CIRCUITS

Delay is another important parameter that can indicate the efficiency of reversible circuits. Here, delay represents the critical delay of the circuit. In many of the earlier works on reversible combinational circuits such as in [26], [12], the delays of each reversible gate such as 2x2, 3x3 and 4x4 reversible gates, all are considered to be of unit delay irrespective of their computational complexity. This is not fair for comparison as delay will vary according to the complexity of a reversible gate. In our delay calculations, we use the logical depth as the measure of the delay [8]. The delays of all 1x1 gate and 2x2 reversible gate are taken as unit delay called Δ . Any 3x3 reversible gate can be designed from 1x1 reversible gates and 2x2 reversible gates, such as the CNOT gate, the Controlled-V and the Controlled- V^+ gates. Thus the delay of a 3x3 reversible gate can be

computed by calculating its logical depth when it is designed from smaller 1x1 and 2x2 reversible gates. Figure 3(b) shows the logic depth in the quantum implementation of Toffoli gate. Thus, it can be seen that the Toffoli gate has the delay of 5 Δ . Each 2x2 reversible gate in the logic depth contributes to 1 Δ delay. Similarly, Peres gate shown in Fig. 4(b) has the logic depth of 4 that results in its delay as 4 Δ .

IV. PROPOSED REVERSIBLE HALF SUBTRACTOR

Before discussing the existing design of quantum half subtractor, the basic working of a half subtractor is illustrated. Let A and B are two binary numbers. The half subtractor performs A-B operation. Table I shows the truth table of the half subtractor. The output of the XOR gate produces the difference between A and B. The output of the AND gate $\bar{A} \cdot B$ produces a Borrow. Thus, the output function will be $Borr = \bar{A} \cdot B$; $Diff = A \oplus B$. In the existing literature, the quantum half subtractor as shown in Fig. 5 is designed from 2 CNOT gates (2 Feynman gates) and 1 Toffoli gate [2]. The design in [2] is the most widely used design of quantum half subtractor [18], [19]. The existing design of the reversible half subtractor in [2] has the quantum cost of 7 and delay of 7 Δ , while the existing design in [1] has the quantum cost of 6 and delay of 6 Δ . In this work, we propose the reversible half subtractor design based on a new quantum implementation of the reversible TR gate. The reversible TR gate is a 3 inputs 3 outputs gate having inputs to outputs mapping as $(P=A, Q=A \oplus B, R = A \cdot \bar{B} \oplus C)$ as shown in Fig.6(a). The implementation of the TR gate with 2x2 reversible gates is shown in Fig. 6(b) which shows that the proposed TR gate has quantum cost of 4 and delay of 4 Δ . It is to be noted that the upper bound on the quantum cost of the TR gate was estimated as 6 in [1].

TABLE I
TRUTH TABLE OF HALF SUBTRACTOR

A	B	Borr	Diff
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

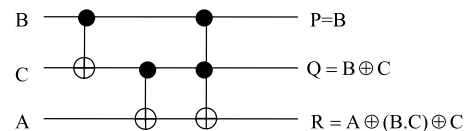


Fig. 5. Existing design for quantum half subtractor [2]

A. Functional Verification of The Quantum Implementation of The TR Gate

We have functionally verified the working of the proposed quantum implementation of the TR gate. The output P of the TR gate is equal to A and the output Q is equal to $A \oplus B$ thus the functionality of the outputs P and Q is easy to verify. The

TABLE II
TRUTH TABLE FOR THE TR GATE

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

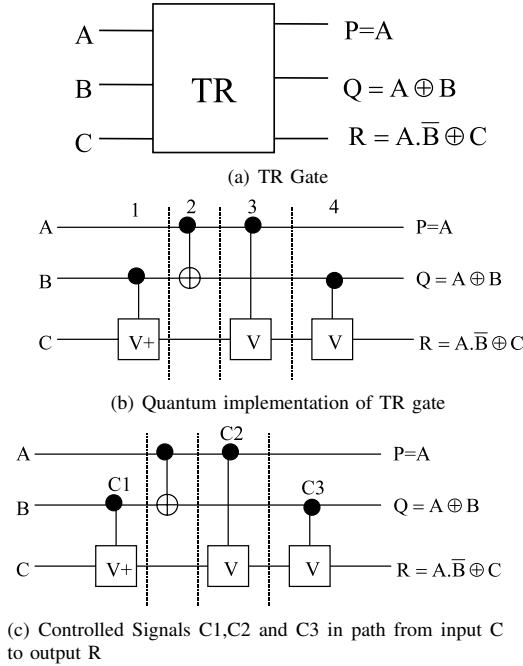


Fig. 6. The TR Gate and its working in various modes

path of the outputs Q consists of V^+ and V gates thus cannot be directly verified. In order to verify the output R, we use the truth table of the TR gate which is shown in Table II, and compare the expected output with the output produced. For the path from input C to output R, the controlled signals of V^+ and V gates are labeled as C1, C2 and C3 as shown in Fig. 6(c). A small illustration of the verification of the output R is shown below for two input combinations in which the inversion and identity properties of V and V^+ gates will be utilized (the properties of V and V^+ gates working as an NOT gate and identity gate are discussed earlier in Section II.B):

- 1) Consider the case when inputs ABC to have value 101. Now we have A=1, B=0 and C=1 thus control signals C1, C2 and C3 will have values as C1=0, C2=1 and C3=1, thus first V^+ gate will not play the controlling role and will just work as a wire transferring the input C. The second and third V gates will be active playing the controlling role resulting in a NOT gate (two V

gates in series work as a NOT gate). Thus at output R we will have the inverted value of C resulting in the value at output R as '0'. From the logic equation the output R is $R = A \cdot \bar{B} \oplus C$ which also produce the value as 0. This verifies the working of the quantum implementation of the TR gate for inputs ABC to have value 101.

- 2) Consider the case when inputs ABC to have value 111, we have A=1, B=1 and C=1 thus control signals C1, C2 and C3 will have values as C1=1, C2=1 and C3=0. The second V gate will not play control role since control signal C3 is 0, the first V^+ and third V^+ gate will form an identity resulting in value of input c passed to output R producing R=C. Thus the output R will be 1. From the logic equation R is $R = A \cdot \bar{B} \oplus C$ which also produce the value as 1. This verifies the working of the quantum implementation of the TR gate for inputs ABC to have value 111. Similarly, the proposed design is tested for all 8 inputs combinations and it matches the expected output.

B. Improved Design of Reversible Half Subtractor

Figure 7(a) shows the working of the TR gate as a reversible half subtractor. As shown in Fig.7(b), the TR gate implements the reversible half subtractor with quantum cost of 4, delay of 4 Δ and 0 garbage outputs (the inputs regenerated at the outputs are not considered as garbage outputs). A comparison of the reversible half subtractors is shown in Table III. Thus proposed design achieves 43% reduction in terms of quantum cost (QC) and delay compared to design presented in [2], while the improvement is 33% in terms of the quantum cost (QC) and the delay compared to design presented in [1].

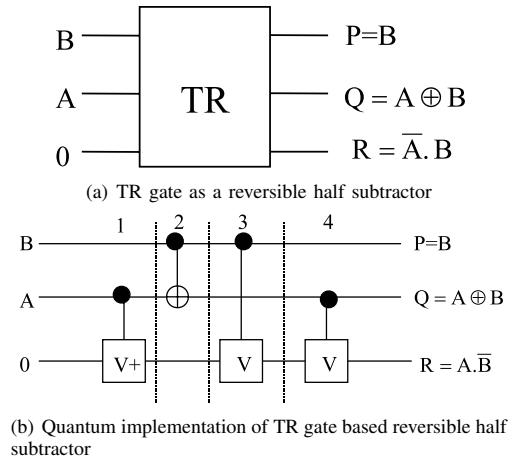


Fig. 7. Improved design of The TR Gate based reversible half subtractor

V. PROPOSED REVERSIBLE FULL SUBTRACTOR

To subtract three binary numbers, one can use a full subtractor which realizes the operation $Y=A-B-C$. The truth table of the full subtractor is shown in Table IV. This

TABLE III
A COMPARISON OF REVERSIBLE HALF SUBTRACTORS

	QC	Delay
Design proposed in [2]	7	7
Design proposed in [1]	6	6
Proposed design	4	4
Improvement in % w.r.t [2]	43	43
Improvement in % w.r.t [1]	33	33

gives the equation of the borrow and difference as follows: $Diff = A \oplus B \oplus C$; $Borr = A \cdot \bar{B} \oplus \bar{A} \oplus B \cdot C$. In the existing literature, the reversible full subtractor is designed with 2 Toffoli gates, 3 Feynman gates and 2 NOT gates [3]. The existing design of reversible full subtractor is shown in Fig. 8. Thus, the existing reversible full subtractor has the quantum cost of 15, delay of 15 Δ . In this work, we propose the design of the reversible full subtractor in Fig.9. It requires two TR gates to design a reversible full subtractor with zero garbage outputs. The quantum realization of the TR gate based reversible full subtractor is shown in Fig. 10(a). From Fig. 10(a), we can see that the TR gate based reversible full subtractor has the quantum cost of 8 with delay of 8 Δ . As can be seen in the Fig. 10(a) the fourth gate (V gate) and the fifth gate (V^+ gate) are in series thus forming an identity and can be removed. This results in a new optimized design of TR gate based reversible full subtractor with quantum cost of 6 and delay of 6 Δ . Thus, compared to the existing design [3], the proposed reversible full subtractor design based on TR gate has an improvement ratio of 60% both in terms of number of quantum cost(QC) and delay, while compared to existing design [1], the improvement is 50% in terms of the quantum cost and the delay. The results are summarized in V.

TABLE IV
TRUTH TABLE OF FULL SUBTRACTOR

A	B	C	Borr	Diff
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

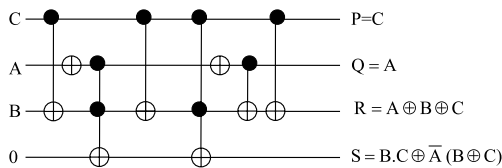


Fig. 8. Existing design of quantum full subtractor [3]

VI. DISCUSSIONS AND CONCLUSIONS

In this work, we have presented efficient designs of reversible subtractors based on the quantum gates imple-

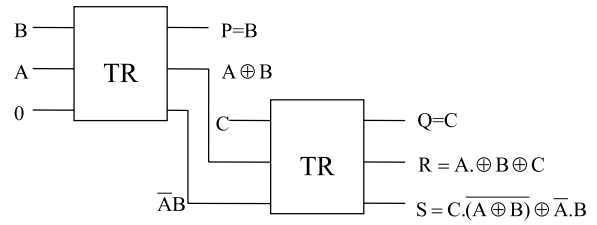
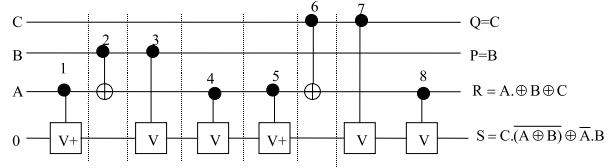
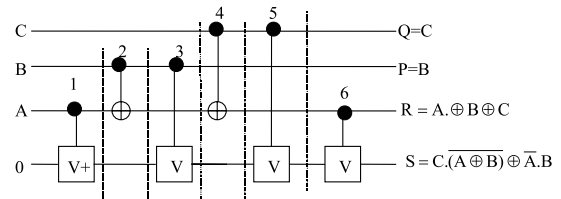


Fig. 9. The TR gate as a full subtractor



(a) Quantum implementation of TR gate based reversible full subtractor



(b) Optimized Quantum implementation of TR gate based reversible full subtractor

Fig. 10. Quantum implementation of TR gate based reversible full subtractor

TABLE V
A COMPARISON OF REVERSIBLE FULL SUBTRACTORS

	QC	Delay
Design proposed in [3]	15	15
Design proposed in [1]	12	12
Proposed Design	6	6
Improvement in % w.r.t [3]	60	60
Improvement in % w.r.t [1]	50	50

mentation of the reversible TR gate. The proposed reversible subtractor designs are shown to be better than the existing designs in terms of the quantum cost and delay while maintaining the minimal number of garbage outputs. We conclude that the design of a specific reversible gate for a particular combinational function can be very much beneficial in minimizing the quantum cost, delay and the garbage outputs. Further, we observe a special property of the reversible TR gate in relation to the popular Peres gate. We derive the inverse of the TR gate since a reversible gate can be combined with its inverse reversible gate to minimize the garbage outputs [20]. In order to derive the logic equations of the inverse TR gate, we performed the reverse mapping of the TR gate outputs working as inputs to generate the inputs of the TR gate. We observe that the inverse of TR gate is same as the existing Peres gate having inputs to outputs mapping as $(P=A, Q=A \oplus B, R = A \cdot B \oplus C)$. Among the existing 3x3 reversible gates, the TR gate and the Peres gate

have the minimum quantum cost. Thus, the proposed TR gate can be combined with its inverse reversible gate (Peres gate) to design minimal quantum cost and garbageless reversible circuits. The proposed efficient designs of reversible subtractors will find applications in emerging nanotechnologies requiring dedicated reversible subtractors units.

REFERENCES

- [1] H. Thapliyal and N. Ranganathan, "Design of efficient reversible binary subtractors based on a new reversible gate," in *Proc. the IEEE Computer Society Annual Symposium on VLSI*, Tampa, Florida, May 2009, pp. 229–234.
- [2] K. V. R. M. Murali, N. Sinha, T. S. Mahesh, M. H. Levitt, K. V. Ramanathan, and A. Kumar, "Quantum information processing by nuclear magnetic resonance: experimental implementation of half-adder and subtractor operations using an oriented spin-7/2 system," *Physical Review A*, vol. 66, no. 2, p. 022313, 2002.
- [3] K.-W. Cheng and C.-C. Tseng, "Quantum full adder and subtractor," *Electronics Letters*, vol. 38, no. 22, pp. 1343–1344, Oct 2002.
- [4] R. Landauer, "Irreversibility and heat generation in the computational process," *IBM J. Research and Development*, vol. 5, pp. 183–191, Dec. 1961.
- [5] C.H. Bennett, "Logical reversibility of computation," *IBM J. Research and Development*, vol. 17, pp. 525–532, Nov. 1973.
- [6] M. A. Nielsen and I. L. Chuang, *Quantum Computation and Quantum Information*. New York: Cambridge Univ. Press, 2000.
- [7] V. Vedral, A. Barenco, and A. Ekert, "Quantum networks for elementary arithmetic operations," *Phys. Rev. A*, vol. 54, no. 1, pp. 147–153, Jul 1996.
- [8] M. Mohammadi and M. Eshghi, "On figures of merit in reversible and quantum logic designs," *Quantum Information Processing*, vol. 8, no. 4, pp. 297–318, Aug. 2009.
- [9] D. Maslov and G. W. Dueck, "Improved quantum cost for n-bit toffoli gates," *IEE Electronics Letters*, vol. 39, no. 25, pp. 1790–1791, Dec. 2003.
- [10] M. Haghparast, S. Jassbi, K. Navi, and O. Hashemipour, "Design of a novel reversible multiplier circuit using hng gate in nanotechnology," *World App. Sci. J.*, vol. 3, no. 6, pp. 974–978, 2008.
- [11] H. Thapliyal and M.B. Srinivas, "Novel reversible multiplier using novel reversible TSG gate," in *Proc. the 4th ACS/IEEE International Conference on Computer Systems and Applications*, Dubai, UAE, 2006, pp. 100–103.
- [12] A. K. Biswas, M. M. Hasan, A. R. Chowdhury, and H. M. Hasan Babu, "Efficient approaches for designing reversible binary coded decimal adders," *Microelectron. J.*, vol. 39, no. 12, pp. 1693–1703, 2008.
- [13] J. W. Bruce, M. A. Thornton, L. Shivakumaraiah, P. S. Kokate, and X. Li, "Efficient adder circuits based on a conservative reversible logic gate," in *Proc. IEEE Symposium on VLSI, 2002*, 2002, pp. 83–88.
- [14] H. Thapliyal and N. Ranganathan, "Design of reversible sequential circuits optimizing quantum cost, delay and garbage outputs," *ACM Journal of Emerging Technologies in Computing Systems*, vol. 6, no. 4, pp. 14:1–14:35, Dec. 2010.
- [15] H. Thapliyal and N. Ranganathan, "Design of efficient reversible logic based binary and bcd adder circuits," *To appear ACM Journal of Emerging Technologies in Computing Systems*, 2011.
- [16] ———, "Reversible logic-based concurrently testable latches for molecular qca," *IEEE Trans. Nanotechnol.*, vol. 9, no. 1, pp. 62–69, Jan. 2010.
- [17] H. Thapliyal, N. Ranganathan, and R. Ferreira, "Design of a comparator tree based on reversible logic," in *Proc. the 10th IEEE International Conference on Nanotechnology*, Seoul, Korea, Aug. 2010, pp. 1113–1116.
- [18] A. N. Al-Rabadi, "Closed-system quantum logic network implementation of the viterbi algorithm," *Facta universitatis-Ser.: Elec. Energ.*, vol. 22, no. 1, pp. 1–33, April 2009.
- [19] I. Oliveira, R. S. Jr., T. Bonagamba, E. Azevedo, and J. C. C. Freitas, *NMR Quantum Information Processing*. Elsevier Science, 2007.
- [20] E. Fredkin and T. Toffoli, "Conservative logic," *International J. Theor. Physics*, vol. 21, pp. 219–253, 1982.
- [21] T. Toffoli, "Reversible computing," MIT Lab for Computer Science, Tech. Rep. Tech memo MIT/LCS/TM-151, 1980.
- [22] A. Peres, "Reversible logic and quantum computers," *Phys. Rev. A, Gen. Phys.*, vol. 32, no. 6, pp. 3266–3276, Dec. 1985.
- [23] J. A. Smolin and D. P. DiVincenzo, "Five two-bit quantum gates are sufficient to implement the quantum fredkin gate," *Physical Review A*, vol. 53, pp. 2855–2856, 1996.
- [24] W. N. Hung, X. Song, G. Yang, J. Yang, and M. Perkowski, "Optimal synthesis of multiple output boolean functions using a set of quantum gates by symbolic reachability analysis," *IEEE Trans. Computer-Aided Design*, vol. 25, no. 9, pp. 1652–1663, Sept. 2006.
- [25] D. Maslov and D. M. Miller, "Comparison of the cost metrics for reversible and quantum logic synthesis," <http://arxiv.org/abs/quant-ph/0511008>, 2006.
- [26] M. Khan, "Design of full-adder with reversible gates," in *Proc. International Conference on Computer and Information Technology*, 2002, pp. 515–519.