

Design of A Reversible Bidirectional Barrel Shifter

Saurabh Kotiyal, Himanshu Thapliyal and Nagarajan Ranganathan
University of South Florida, Tampa, FL, USA
Email: {skotiyal, hthapliy, ranganat}@cse.usf.edu

Abstract—Reversible logic has promising applications in the field of quantum computing, optical computing, low power computing, and other emerging computing technologies. A barrel shifter that can shift and rotate multiple bits in a single cycle is an important component of many computing units. This paper presents the reversible design of bidirectional arithmetic and logical barrel shifter. The proposed design consists of the reversible Fredkin and Feynman gates. The Fredkin gate used in the design of reversible bidirectional arithmetic and logical barrel shifter can implement the 2:1 MUX with minimum quantum cost, minimum number of ancilla bits and minimum number of garbage outputs while the Feynman gate is used to avoid the fanout as fanout is not allowed in the reversible logic. The design is evaluated in terms of number of garbage outputs, quantum cost and number of ancilla bits.

I. INTRODUCTION

In reversible logic there exists a one to one mapping between the inputs and the outputs vectors. In an irreversible circuit erasing a bit is equivalent to dissipation of $kT \ln 2$ joules of heat energy where k is the Boltzmann's constant and T is the absolute temperature of environment [1]. If the operations are performed in reversible manner based on reversible logic circuits then there won't be dissipation of $kT \ln 2$ joules of heat energy [2]. The reversible circuits can be designed using the reversible logic gates. Reversible logic also has the applications in emerging nanotechnologies such as quantum dot cellular automata, optical computing, quantum computing and low power computing, etc. The major application of reversible logic is in the quantum computing [3], [4]. A quantum computer will be viewed as a quantum network (or family of quantum networks) consisting of quantum logic gates, where each gate performing an elementary unitary operation on one, two or more two-state quantum system called qubits. Quantum networks must be built from reversible logical components [5]. The reversible circuits have associated overhead in terms of number of ancilla inputs and the number of garbage outputs. An auxiliary constant input used to design a reversible circuit is called the ancilla input bit [6], while the outputs which do not perform any useful operation and needed to maintain reversibility of the circuit are termed as garbage outputs. An efficient design of reversible circuit is optimized in terms of number of garbage outputs, number of ancilla inputs and the quantum cost. A (n, k) barrel shifter is a combinational circuit with n inputs and n outputs where k select lines controls the shift operation. The barrel shifter can shift and rotate multiple bits in a single cycle and is an important part of digital signal processors [7], [8]. In the existing literature there exist designs of

the reversible barrel shifters that can only perform the left rotate operation [9], [10]. Researchers have also proposed the design of reversible sequential shift registers [11]. As the reversible barrel shifter can shift and rotate multiple bits in a single cycle and thus will be considerably faster than the reversible sequential shift register, this paper presents the reversible design of bidirectional arithmetic and logical barrel shifter. The proposed design of reversible bidirectional arithmetic and logical barrel shifter can perform logical right shifting, arithmetic right shifting, logical left shifting and arithmetic left shifting operations. The reversible Fredkin and Feynman gates are the basic building blocks of our proposed design.

The structure of the paper is as follows: Section II explains the basic reversible gates; Section III presents the introductory material on barrel shifters; Section IV shows the proposed design of the reversible bidirectional arithmetic and logical barrel shifter. In Section V, the performance analysis of the proposed shifter is illustrated. Section VI provides the conclusions.

II. BASIC REVERSIBLE GATES

Several reversible gates such as the Toffoli gate, the Fredkin gate, the Peres gate and the TR gate exists in the literature [12], [13], [14], [15]. The quantum cost of reversible gate is the number of 1x1 and 2x2 reversible gates needed to design a 3x3 reversible gate. The quantum cost of all 1x1 and 2x2 reversible gates are considered as unity [16], [3], [17]. The 3x3 reversible gates are designed from 1x1 NOT gate, and 2x2 reversible gates such as Controlled-V and Controlled-V+ (V is a square-root of NOT gate and V+ is its hermitian), the Feynman gate which is also known as Controlled NOT gate.

A. The NOT Gate

A NOT gate is 1x1 gate represented as shown in Fig. 1(a). Since it is a 1x1 gate, its quantum cost is unity.

B. Controlled-V and Controlled-V+ Gates

A controlled-V gate is shown in Fig. 1(b). In a controlled-V gate, when the control signal $A=0$ then the qubit B will pass through the controlled part unchanged, i.e., we will have $Q=B$. When the value of $A=1$ then the unitary operation $V = \frac{i+1}{2} \begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}$ is applied to input B, i.e., $Q=V(B)$. The controlled-V+ gate is shown in Fig. 1(c). In the controlled-V+ gate when the control signal $A=0$ then the qubit B will pass through the controlled part unchanged, i.e., we will have

$Q=B$. When $A=1$ then the unitary operation $V^+ = V^{-1}$ is applied to the input B, i.e., $Q=V^+(B)$.

The V and V^+ quantum gates have the following properties:

$$\begin{aligned} V \times V &= NOT \\ V \times V^+ &= V^+ \times V = I \\ V^+ \times V^+ &= NOT \end{aligned}$$

The property as shown above represents that when two V gates are in series they will behave as a NOT gate. Similarly two V^+ gate in series behaves as a NOT gate. A V gate in series with a V^+ gate and vice versa, is an identity. The more details of V and V^+ gate can be found in [5], [3].

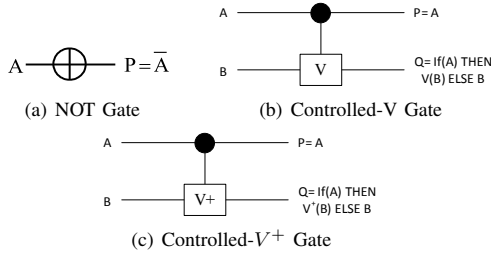


Fig. 1. NOT, Controlled-V and Controlled- V^+ Gates

C. Feynman Gate (CNOT Gate)

The Feynman gate (FG) or the controlled-NOT gate (CNOT) is a 2-inputs and 2-outputs reversible gate with the mapping (A, B) to (P=A, Q=A \oplus B). Here A is the controlling input and B is the controlled input; P, Q are the two outputs. Since the Feynman gate is a 2x2 reversible gate, it has a quantum cost of 1. Figure 2(a) and 2(b) shows the block diagram and the quantum representation of the Feynman gate. Fanout is not allowed in reversible logic. Feynman gate is helpful in this regard as it can be used for copying the signal thus avoiding the fanout problem as shown in Fig. 2(c). It can also be used for generating the complement of a given input signal as shown in Fig. 2(d).

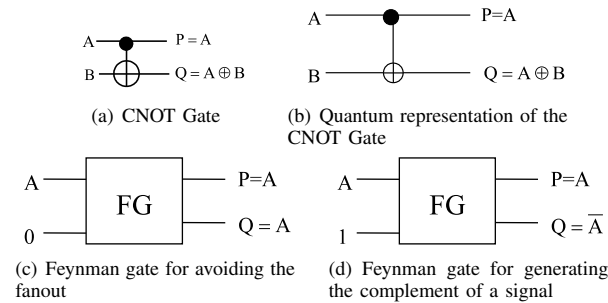


Fig. 2. CNOT gate, its quantum implementation and its useful properties

D. Fredkin Gate

Fredkin gate is a 3x3 reversible logic gate with three inputs and three outputs. Figure 3(a) shows the block diagram of a Fredkin gate. The Fredkin gate maps (A, B, C) to (P=A, Q =

$\bar{A}B+AC, R = AB+\bar{A}C$), where A, B, C are the inputs and P, Q, R are the outputs, respectively [18]. A Fredkin gate can work as 2:1 MUX, as it is able to swap its other two inputs depending on the value of its first input. Referring the Fig. 3(a), the first input A works as a controlling input while the inputs B and C work as controlled inputs. Thus when $A=1$ the inputs B and C will be swapped resulting in the value of the outputs as $Q=C$ and $R=B$. If $A=0$ the outputs P and Q will be directly connected to inputs A and B. Figure 3(b) shows the quantum implementation of a Fredkin gate with a quantum cost of 5 [3]. In Fig. 3(b) each dotted rectangle is equivalent to a 2x2 Feynman gate and the quantum cost of each dotted rectangle is considered as 1 [16]. The same assumption is used for calculating the quantum cost of the Fredkin gate in [3]. Thus, the quantum cost of the Fredkin gate is 5 as it consists of 2 dotted rectangle, 1 Controlled-V gate and 2 CNOT gate. In this work, we have also followed the assumption by [16], and in our quantum cost calculations the quantum cost of the Fredkin gate is considered as 5.

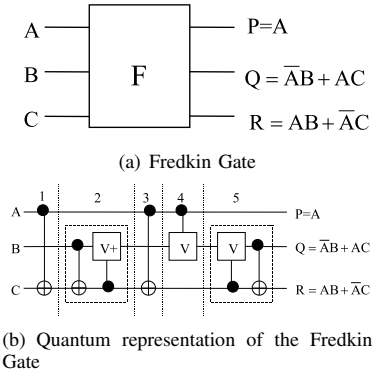


Fig. 3. Fredkin Gate and its quantum implementation

III. BARREL SHIFTER

A Barrel shifter is a n inputs and n outputs combinational logic circuit in which k select lines controls the bit shift operation. Barrel shifter can be unidirectional allowing data to be shifted only to left (or right), or bi-directional which provides data to be rotated or shifted in both the directions. A barrel shifter having n inputs and k select lines is called (n,k) barrel shifter. Among the different designs of barrel shifter, the logarithmic barrel shifter is most widely used because of its simple design, less area and the elimination of the decoder circuitry. The conventional irreversible design of a logarithmic barrel shifter is shown in Fig. 4. A n-bit Logarithmic Barrel Shifter contains $\log_2(n)$ stage where the i_{th} stage either shifts over 2^i bits or leaves the data unchanged. Each stage of a logarithmic barrel shifter is controlled by a control bit. If the control bit is set to one then the input data will be shifted in the associated stage else it remains unchanged. The proposed work presents the designs of reversible bidirectional arithmetic and logical barrel shifter that can perform six operations: logical right shift, arithmetic

right shift, right rotate, logical left shift, arithmetic left shift and left rotate.

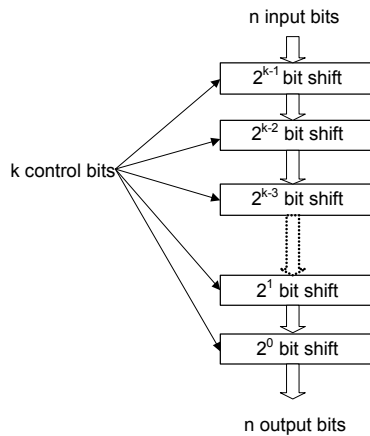


Fig. 4. Structure of (n, k) logarithmic barrel shifter

IV. DESIGN OF A REVERSIBLE BIDIRECTIONAL ARITHMETIC AND LOGICAL BARREL SHIFTER

We present the reversible design of bidirectional arithmetic and logical barrel shifter. The proposed design of reversible bidirectional arithmetic and logical barrel shifter can perform logical right shifting, arithmetic right shifting, logical left shifting and arithmetic left shifting operations. The proposed design approach is illustrated with an example of a (8,3) reversible bidirectional arithmetic and logical barrel shifter as shown in Fig. 5. All operations that can be performed by a (8,3) reversible bidirectional arithmetic and logical shifter are shown in Table I for different values of control signals sra , sla and $left$. As explained in Table I, the barrel shifter performs the various operations such as logical right shift, logical left shift etc. depending on the values of sra , sla and $left$ control signals. In the proposed design, the input data is represented as $i_7, i_6, i_5, i_4, i_3, i_2, i_1, i_0$ while the shift value is controlled by select signals represented as $S_2 S_1 S_0$.

The design of a reversible arithmetic and logical barrel shifter can be divided into four modules: (i) Data reversal control unit-I, (ii) Arithmetic right shift control unit, (iii) Shifter unit which consists of three sub-modules that performs Stage I, Stage II and Stage III operations discussed later, (iii) Arithmetic left shift control unit, (iv) Data reversal control unit-II. The reversible design of the modules of the reversible bidirectional arithmetic and logical barrel shifter along with their working are explained as follows:

TABLE I
OPERATION PERFORMED BY A (N,K) REVERSIBLE BIDIRECTIONAL ARITHMETIC AND LOGICAL BARREL SHIFTER

Operation performed	Control signal values		
Logical right shift	$sra=0$	$sla=0$	$left=0$
Arithmetic right shift	$sra=1$	$sla=0$	$left=0$
Logical left shift	$sra=0$	$sla=0$	$left=1$
Arithmetic left shift	$sra=0$	$sla=1$	$left=1$

1) *Data Reversal Control Unit-I*: The direction of the shift operation performed on reversible arithmetic and logical barrel shifter is controlled by the control signal $left$ as can be seen in the Table I. For the value of control signal $left$ as 1, the reversible bidirectional arithmetic and logical barrel shifter performs the shift operation in the left direction, that is, the arithmetic left shift operation or logical left shift operation. Otherwise, for the value of $left=0$ the shift operation is performed in the right direction, that is, arithmetic right shift operation or logical right shift operation. The data reversal control unit-I has Fredkin gates as the key components, since two outputs of the Fredkin gate can work as 2:1 MUXes. By utilizing two outputs of the Fredkin gate as 2:1 Muxes, 4 Fredkin gates can be used to reverse the 8 bit input data. After observing the behavior of right shift and left shift operation. We noticed that for a n bit input data a left shift operation by k-bit can be performed in three steps : (i) reverse the input data, (ii) perform k bit right shift operation, and (iii) reverse the outputs of the step (ii). For example, for a 8-bit input data $i_7, i_6, i_5, i_4, i_3, i_2, i_1, i_0$ the three steps of logical left shift operation by 3 bits will be: (i) reverse $i_7, i_6, i_5, i_4, i_3, i_2, i_1, i_0$ to produce $i_0, i_1, i_2, i_3, i_4, i_5, i_6, i_7$, (ii) perform the 3 bit logical right shift operation to produce $0, 0, 0, i_0, i_1, i_2, i_3, i_4$, and (iii) reverse the outputs of step (ii) to yield $i_4, i_3, i_2, i_1, i_0, 0, 0, 0$. The date reversal control unit-I is shown in Fig. 5.

2) *Arithmetic Right Shift Control Unit*: The arithmetic right shift control unit controls the arithmetic right shift operation. This unit is designed using a single Fredkin gate controlled by the control signal sra , and preserves the sign bit of input data. If the value of control signal $sra = 1$, the arithmetic right shift operation is performed otherwise it simply passes the data to the next module. As fanout is not allowed in reversible logic multiple copies of the sign bit are created using the Feynman gates. The reversible arithmetic right shift control unit is shown in Fig.5.

3) *Shifter Unit*: The shifter unit in the design of reversible bidirectional arithmetic and logical shifter is responsible for the amount of shift operation performed. This unit is controlled by the control signals S_2, S_1 and S_0 . The shifter unit can be divided into three stages. All the three stages are designed using the chain of 8 Fredkin gates controlled by the control signals S_2, S_1 and S_0 . The first, second and the third stages of the shifter unit right shifts the input data by $2^2, 2^1$ and 2^0 bits depending on the value of control signal S_2, S_1 and S_0 , respectively. Fig. 5 shows the three stage design of the reversible shifter unit. The Feynman gates are used in the design to avoid the fanout problem. The working of the three stages of the shifter unit is explained as follows:

- *Stage – I* : The first stage of shifter unit is re-

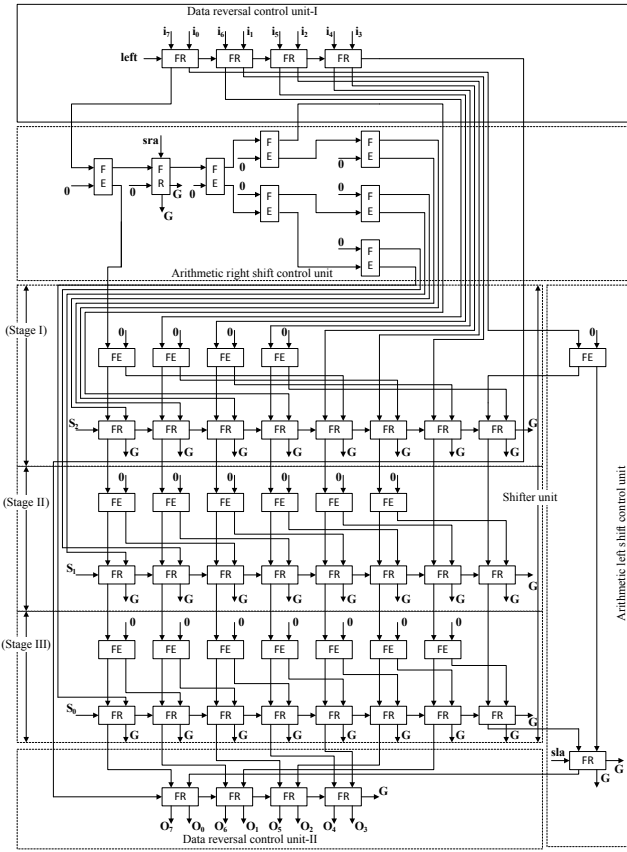


Fig. 5. Proposed (8,3) reversible bidirectional arithmetic and logical barrel shifter *FE represents Feynman Gates, FR represents Fredkin gates and G represents the garbage outputs * Number of garbage outputs=32 * Number of ancilla bits=26

sponsible for shifting the input data by 2^2 -bits and is controlled by the control signal S_2 . If the value of control signal S_2 is 1 the input data is right shifted by 2^2 -bits, else the input data remains unchanged. The outputs of the Stage I is passed as inputs to Stage II of the shifter unit.

- *Stage – II* : The second stage of the shifter unit works on the outputs of the first stage and is controlled by the control signal S_1 . If the value of control signal S_1 is 1 the input data provided to the second stage is right shifted by 2^1 -bits, else the input data remains unchanged. The outputs of the Stage II is passed as inputs to Stage III of the shifter unit.
- *Stage – III* : The third stage of the shifter unit is controlled by the control signal S_0 . If the value of control signal S_0 is 1 the output data generated by the stage-II is right shifted by 2^0 -bits else the output data remains unchanged. The outputs of this stage is passed as inputs to the next module in the design of reversible bidirectional arithmetic and logical shifter.

- 4) *Arithmetic Left Shift Control Unit*: The design of the arithmetic left shift control unit is similar to the design

of the arithmetic right shift control unit. This control unit is responsible to perform the arithmetic left shift operation, and is controlled by the control signal sla . This unit is implemented using a single Fredkin gate. If the value of control signal $sla = 1$ this unit preserves the sign bit needed to perform the arithmetic left shift operation, else it simply passes the LSB of the shifter unit. The arithmetic left shift control unit is shown in the Fig. 5.

- 5) *Data Reversal Control Unit II*: The design of this unit is same as explained for data reversal control unit I and is shown in Fig. 5. The data reversal control unit II reverses its 8 bit input which consists of 7 bits from the outputs of the shifter unit and 1 bit from the output of the arithmetic left shift control unit. The data reversal control unit is controlled by the control signal $left$. If the value of control signal $left$ is 1, this unit reverses its input data to generate a left shifted result else it simply passes the input data to its outputs.

The proposed method illustrated above to design a (8,3) reversible bidirectional arithmetic and logical barrel shifter can be generalized to design a (n,k) reversible bidirectional arithmetic and logical barrel shifter. The (8,3) reversible bidirectional arithmetic and logical barrel shifter uses 25 Feynman gate to copy the input data to avoid the fanout, and 34 Fredkin gates are used for arithmetic and logical bidirectional shifting. Below we summarize the important characteristics of the proposed (n,k) reversible bidirectional arithmetic and logical shifter on the basis of garbage outputs, ancilla bits and the quantum cost.

V. PERFORMANCE EVALUATION

To design a (n,k) reversible bidirectional arithmetic and logical shifter, the Feynman gates are used for copying the input data. It is to be noted that in the proposed design Feynman gate is only used to avoid the fanout problem. The data reversal unit-I and data reversal unit-II consist of chains of $n/2$ Fredkin gates. The shifter unit at each stage requires 2^{k-m} for $m = 0$ to $(k-1)$ number of Feynman gates and chain of n Fredkin gates. The arithmetic right shift control unit uses one Fredkin and $2^k - 1$ Feynman gates. The arithmetic left shift control unit requires one Fredkin gate and one Feynman gate. Thus the total number of Feynman gates used to design a (n,k) reversible bidirectional arithmetic and logical shifter is:

$FE = \text{Number of Feynman gates required to design arithmetic right shift control unit} + \text{number of Feynman gates used in shifter control unit} + \text{number of Feynman gates used in arithmetic left shift control unit} = \sum_{m=0}^{k-1} (n - 2^m) + (2^k - 1) + 1 = 2^k + \sum_{m=0}^{k-1} (n - 2^m)$.

The total number of Fredkin gates used to design a (n,k) reversible bidirectional arithmetic and logical shifter can be written as:

$FR = \text{Number of Fredkin gates used in data reversal control unit-I} + \text{Number of Fredkin gates used in arithmetic right shift control unit} + \text{Number of Fredkin gates used in shifter unit} + \text{Number of Fredkin gates used in arithmetic left shift}$

control unit +Number of Fredkin gates used in data reversal control unit-II= $n/2 + 1 + (n * k) + 1 + n/2 = n * (k + 1) + 2$.

A. Garbage Outputs

The shifter unit in the design of (n,k) reversible bidirectional arithmetic and logical shifter can be designed in k stages and each stage consists of the chain of n Fredkin gates to perform the shift operation. Each Fredkin gate in the chain of n Fredkin gates produces atleast one garbage output except the last Fredkin gate which produces two garbage outputs. Further, each Fredkin gate used in the design of arithmetic right shift control unit and arithmetic left shift control unit produces two garbage outputs. The last Fredkin gate of the data reversal control unit-II produces one garbage output as the control signal *left* cannot be utilized further. Hence the number of garbage outputs (GOs) required to design a (n,k) reversible bidirectional arithmetic and logical shifter can be written as $GOs = k(n + 1) + 5$. Table II shows the number of garbage outputs produced for different reversible bidirectional arithmetic and logical barrel shifter designs. In the table, n is the number of input data bits and k represents the shift value. It can be seen that the number of garbage outputs in (8,3) reversible bidirectional arithmetic and logical barrel shifter design that was illustrated in Fig. 5 are 32 which matches with the result in Table II.

TABLE II
GARBAGE OUTPUTS IN (N,K) REVERSIBLE BIDIRECTIONAL ARITHMETIC AND LOGICAL BARREL SHIFTER

n/k	n=4	n=8	n=16	n=32	n=64
k=2	15	23	39	71	135
k=3		32	56	104	200
k=4			73	137	265
k=5				170	330
k=6					395

B. Ancilla input Bits

A (n,k) reversible bidirectional arithmetic and logical barrel shifter can be designed using $2^k + \sum_{m=0}^{k-1} (n - 2^m)$ Feynman gates. Each Feynman gate requires one ancilla input bit to copy the input data. Additionally, the Fredkin gate used in arithmetic right shift control unit requires one ancilla bit. Thus the total number of ancilla inputs (ANs) required to design a (n,k) reversible bidirectional arithmetic and logical barrel shifter is $ANs = 2^k + \sum_{m=0}^{k-1} (n - 2^m) + 1$. The table III shows the number of ancilla bits required to design a reversible bidirectional arithmetic and logical barrel shifter for different values of n and k. It can be seen from the Table III that the total number of ancilla inputs to design a (8,3) reversible bidirectional arithmetic and logical barrel shifter are 26 which is same as illustrated in Fig. 5.

C. Quantum Cost

The quantum cost of (n,k) reversible bidirectional arithmetic and logical shifter depends on the number of Feynman and Fredkin gates used. As the quantum cost of the Feynman gate is considered as one, while the

TABLE III
ANCILLA INPUTS IN (N,K) REVERSIBLE BIDIRECTIONAL ARITHMETIC AND LOGICAL BARREL SHIFTER

n/k	n=4	n=8	n=16	n=32	n=64
k=2	10	18	34	66	130
k=3		26	50	98	194
k=4			66	130	258
k=5				162	322
k=6					386

quantum cost of the Fredkin gate is considered as five, the quantum cost of the proposed design of (n,k) reversible bidirectional arithmetic and logical shifter can be written as $QuantumCost = 5 * (number\ of\ Fredkin\ gates) + (number\ of\ Feynman\ gates)$. The quantum cost(QC) of the (n,k) reversible bidirectional arithmetic and logical barrel shifter can be represented as $QC = 5 * (n * (k + 1) + 2) + 2^k + \sum_{m=0}^{k-1} (n - 2^m)$. Table IV shows the quantum cost for a reversible bidirectional arithmetic and logical shifter for different n and k values. The quantum cost of a (8,3) reversible bidirectional arithmetic and logical shifter shown in Fig. 5 is 195.

TABLE IV
QUANTUM COST OF (N,K) REVERSIBLE BIDIRECTIONAL ARITHMETIC AND LOGICAL BARREL SHIFTER

n/k	n=4	n=8	n=16	n=32	n=64
k=2	79	147	283	555	1099
k=3		195	379	747	1483
k=4			475	939	1867
k=5				1131	2251
k=6					2635

VI. CONCLUSIONS

In this paper a novel architecture of a reversible bidirectional arithmetic and logical shifter has been proposed. The proposed bidirectional shifter is designed using Fredkin gates and Feynman gates. The design of bidirectional shifter is been evaluated in terms of garbage outputs, ancilla inputs and the quantum cost. The functional verification of the proposed design of the reversible barrel shifters are performed through simulations using the Verilog HDL flow for reversible circuits illustrated in [15]. We observed that the number of garbage outputs, the number of ancilla inputs and the quantum cost of the (n,k) reversible bidirectional arithmetic and logical barrel shifter increase more rapidly by varying n and keeping k as a constant compared to the reversible bidirectional arithmetic and logical barrel shifter designs in which n is kept as a constant while k is varied.

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