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Design of A Ternary Barrel Shifter Using Multiple-Valued Reversible Logic

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Abstract— **Multiple-valued reversible logic is emerging as a promising computing paradigm as it helps in reducing the width of the reversible or quantum circuits. Further, a barrel shifter that can shift and rotate multiple bits in a single cycle forms the essence of many computing systems. In this paper, we propose an efficient architecture and design of a reversible ternary barrel shifter. The ternary barrel shifter is realized using the Modified Fredkin gates (MFG) and the ternary Feynman gates. The design is evaluated in terms of quantum cost, the number of garbage outputs and the number of ancilla bits. To our knowledge, the use of multiple valued reversible logic for the design of a barrel shifter is being attempted for the first time in the literature.**

Keywords- Modified Fredkin Gate; Quantum cost, Ancilla bits

I. INTRODUCTION

Reversible logic is a promising technology in which there is a one to one mapping between the input and the output vectors. According to Landauer[1], if a system is irreversible then a bit erasing causes *kTln2* joules of heat energy where k is the Boltzmann's constant and T is the absolute temperature of the environment. This *kTln2* joules of heat energy won't be dissipated if a computation is carried reversibly based on reversible logic circuits [13]. Reversible logic has extensive applications in emerging technologies such as quantum computing, quantum dot cellular automata, optical computing, etc [11, 12, 15]. The major application of reversible logic lies in quantum computing. A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; each gate performing an elementary unitary operation on one, two or more two-state quantum systems called qubits. Quantum networks must be built from reversible logical components [2]. Multiple-valued logic (MVL) helps in reducing the width of reversible or quantum circuit. Among multiple-valued quantum logic (MVQL), ternary quantum logic is most widely used [6]. In one of the fundamental contribution [3], it was shown that the basic operations in a multiple valued quantum logic circuits can be performed by conditional two qudit logic gate called Muthukrishnan-Stroud gate (M-S gate). M-S gate is physically realizable with existing ion-trap technology and is useful for implementing ternary reversible gates. Further, barrel shifter that can shift and rotate multiple bits in a single cycle forms the essence of many computing systems such as digital signal processors [14]. In this work, we propose reversible realization of a ternary barrel shifter using ternary Feynman gates and Modified Fredkin gates (MFG) [4]. In the existing literature, there exists reversible design of binary barrel shifter [5], but to the best of our knowledge, the proposed work is first towards the design of the reversible ternary barrel shifter.

In reversible circuits, garbage outputs refers to the outputs, which do not perform any useful operations and are needed to maintain reversibility. An auxiliary constant input is called an ancilla bit[9]. In this work, the reversible ternary barrel shifter is evaluated in terms of quantum cost, number of garbage outputs and the number of ancilla bits. *We have defined the quantum cost of a ternary reversible gate as the number of Muthukrishnan-Stroud gates (M-S gates) and shift gates required in its implementation*. The multiple-valued reversible logic circuit with minimal number of garbage outputs, minimal quantum cost and minimum number of ancilla bits is considered as an efficient design.

The structure of the paper is as follows: Section II explains the basic ternary reversible gates. Section III presents the introductory material on barrel shifters; Section IV shows the proposed design of the reversible ternary barrel shifter. In Section V, the performance analysis of the proposed shifter is illustrated. Section VI provides the conclusions.

II. TERNARY REVERSIBLE GATES

Ternary (three valued) or trivalent logic is an example of multi-valued logic in which the states are $|0\rangle$, $|1\rangle$ and $|2\rangle$. A ternary logic circuit is reversible if there is a unique mapping between the inputs and the output vectors [10]. In this work, we have used ternary Feynman gates and the ternary Modified Fredkin gates (MFG) to design the ternary barrel shifter. It is possible to implement a ternary reversible gate using Muthukrishnan-Stroud gates (M-S gates) [6].

A. *Ternary Feynman Gate*

A ternary Feynman gate is a 2-input and 2-output ternary reversible gate with mapping (A, B) to (P=A, Q=A+B) where A is the controlling input and B is the controlled input. The input A is directly passed to the output P, while the output Q is GF(3) sum of inputs A and B. Figure 2 shows the Feynman gate. The input A can be copied to the outputs P and Q if the value of input B is hardwired to 0. This helps in the use of the Feynman gate to avoid the fan-out. Fan-out is not allowed in reversible logic [7].

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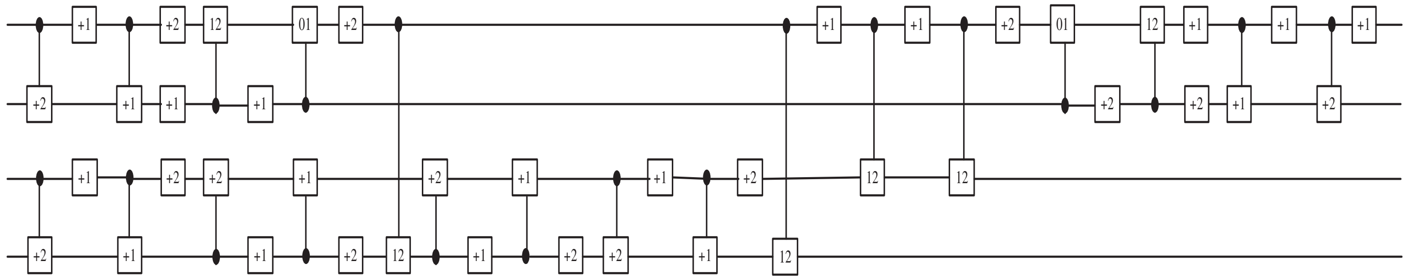

Figure 1. Modified Fredkin gate realization by M-S gates [6]

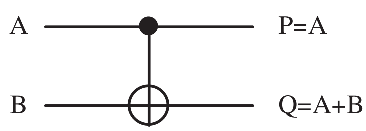

Figure 2. Ternary Feynamn gate

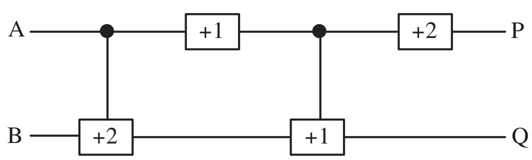

Figure 3. Ternary Feynman gate realization by M-S gates [6]

A ternary Feynman Gate can be realized using two M-S and two shift gates [6], thus it will have the quantum cost of 4. The implementation of ternary Feynman gate using M-S gate is shown in Fig. 3.

B. *Modified Fredkin Gate*

Fredkin gate was introduced for binary reversible logic by Toffoli and Fredkin [8] and is one of the fundamental gates in reversible and quantum computing. In [4], Picton introduced Modified Fredkin gate (MFG) for multi-valued reversible logic. MFG gate is 4*4 reversible gate, having mapping (*A, B, C, D*) to (*P=A, Q=B, R=C if A<B else R=D, S=D if A<B else S=C*), where *A, B, C, D* are the inputs and *P, Q, R, S* are the respective output. The MGF gates swaps the input *C* and *D* if the value of *A>=B* else they remains unchanged. Considering a variable *K=A<B*, the outputs *R* and *S* of the Modified Fredkin gate can be written as $R = \overline{K} \cdot D + KC$ and $S = \overline{K} \cdot C + KD$. Thus, MFG gate has two of its outputs working as 2:1 MUX. Figure 4 shows a 4*4 Modified Fredkin gate.

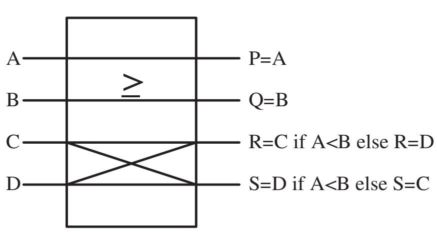

Figure 4. Modified Fredkin Gate

The Modified Fredkin Gate can be implemented using 20 M-S and 21 shift gates [6], thus it will have the quantum cost of 41. The MS gates and shift gates based implementation of the Modified Fredkin gate is shown in Fig. 1.

III. Barrel Shifter

A Barrel shifter is an n inputs and n outputs combinational logic circuit in which k select lines controls the bit shift operation. Barrel shifter can be unidirectional allowing data to be shifted only to left (or right), or bi-directional which provides data to be rotated/shifted in both directions. A barrel shifter having n inputs and k select lines is called (n, k) barrel shifter. According to [5], among several barrel shifter architectures the logarithmic barrel shifter is more efficient in terms of design as well as area and it does not need any decoder circuitry. A simple design of a logarithmic barrel shifter is shown in Fig.5.

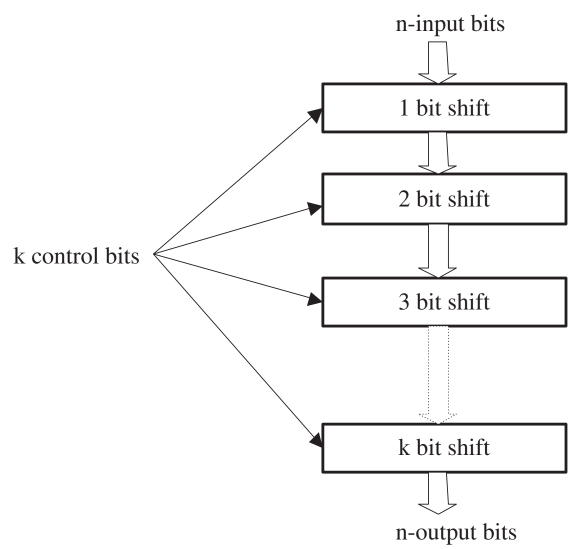

Figure 5. Structure of a (n, k) logarithmic barrel shifter

A Logarithmic Barrel Shifter contains $log_2(n)$ stage where the i_{th} stage either shifts over 2^{i} or passes the data unchanged. Each stage of a logarithmic barrel shifter is controlled by a control bit. If the control bit is set to one then the input data will be shifted in the associated stage else it remains unchanged.

IV. REVERSIBLE TERNARY BARREL SHIFTER

The logarithmic barrel shifter can be implemented using the multiplexers which in turn can be realized using the 2:1 multiplexers. We choose MFG gate to design the reversible ternary logarithmic barrel shifter as two of its outputs (*R* and *S*) can work as ternary 2:1 MUXs that are controlled by two of its inputs *A* and *B*. The ternary Feynman gate is used to avoid the fan-out as fan-out is not allowed in reversible logic. In order to illustrate the design strategy for designing the reversible ternary logarithmic barrel shifter, the design of reversible (4:2) ternary barrel shifter is explained. The (4:2) barrel shifter has four inputs i_0 to i_3 and four outputs O_0 to O_3. The design has two stages, which are controlled by two select signals S_0 and S_1. The logic equations of both the stages are illustrated in the Fig.6 in which K_0 to K_3 represents the intermediate outputs generated at the stage 1, while the final outputs O_0 to O_3 are generated at the stage 2.

Stage1:

$$K_3 = \overline{S_0} \cdot i_3 + S_0 \cdot i_0$$
$$K_2 = \overline{S_0} \cdot i_2 + S_0 \cdot i_3$$
$$K_1 = \overline{S_0} \cdot i_1 + S_0 \cdot i_2$$
$$K_0 = \overline{S_0} \cdot i_0 + S_0 \cdot i_1$$

Stage2:

$$O_3 = \overline{S_1} \cdot K_3 + S_1 \cdot K_1$$
$$O_2 = \overline{S_1} \cdot K_2 + S_1 \cdot K_0$$
$$O_1 = \overline{S_1} \cdot K_1 + S_1 \cdot K_3$$
$$O_0 = \overline{S_1} \cdot K_0 + S_1 \cdot K_2$$

Figure 6. Logic equations of two stages in (4:2) barrel shifter

The equivalent reversible ternary design of the stage 1 and stage 2 is illustrated in Fig.7. The four Feynman gates at the top create copies of the input signals i_0 to i_3 thus avoiding the fan-out. As can be seen from the equations of stage 1 in Fig.6, it needs the chain of four 2:1 MUXs. Thus in the equivalent reversible design shown in Fig.7, first stage is designed from chain of MFG gates working as 2:1 multiplexers. The garbage outputs are minimized by reusing the signals *0* and S_0 regenerated at the outputs *P* and *Q* of the MFG gates, respectively. Thus in the first stage for each MFG gate only output *R* is the garbage output while *S* output generates K_0 to K_3 intermediate outputs. In the second stage that has S_1 as the select signal, we carefully observed that $O_3 = \overline{S_1} \cdot K_3 + S_1 \cdot K_1$ and $O_1 = \overline{S_1} \cdot K_1 + S_1 \cdot K_3$ can be mapped to the same MFG gate at its outputs *S* and *R* instead of using two MFG gates for mapping them. Similarly, $O_2 = \overline{S_1} \cdot K_2 + S_1 \cdot K_0$ and $O_0 = \overline{S_1} \cdot K_0 + S_1 \cdot K_2$ can be mapped to the outputs *R* and *S* of another MFG gate. This process of mapping two outputs signals to one MFG gate (for example, O_3 and O_1) helps in reducing the quantum cost, garbage outputs and number of ancilla bits in the design.

The first stage in the proposed reversible ternary barrel shifter shifts/rotates the input data by 0 or 1 position and the second stage shifts/rotates the input data by 0 or 2 position. Thus the proposed (4:2) reversible ternary shifter provides shift/ rotates of input data by 0, 1, 2 or 3 positions. For an example if the value of S_0S_1=11 then the ternary (4:2) reversible barrel shifter will be able to shift the input data with $2^0 + 2^1$=3 times to the left. Thus having the input data as $i_0i_1i_2i_3$, in the first stage the generated output is $i_1i_2i_3i_0$, which is shift/rotate by one. In the second stage the final output is rotated by two, which is $i_3i_0i_1i_2$. If the value of control bit S_0S_1=00 then the input data remains same (no shift). The illustrated method can be generalized for designing (n,k) reversible ternary barrel shifter. We derive the generalized cost of (n,k) reversible ternary barrel shifter.

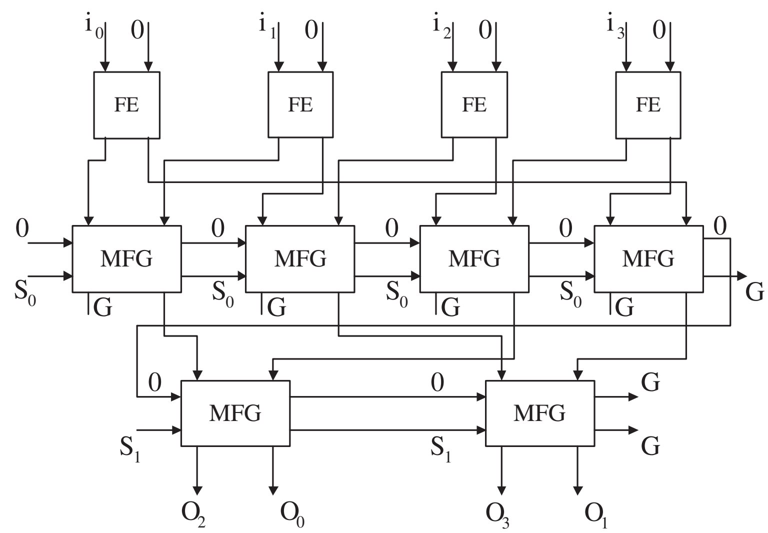

Figure 7. (4:2) Reversible ternary barrel shifter

The proposed (4:2) reversible ternary barrel shifter as shown in Fig. 7 uses 4 ternary Feynaman Gates for producing the fan-out and 6 MFG gates to shift/rotate the input data. Below we summarize the important characteristics of the proposed (n,k) reversible ternary barrel shifter on the basis of garbage outputs, ancilla bits and the quantum cost.

V. PERFORMANCE EVALUATION

In the design of the reversible ternary barrel shifter, the ternary Feynman gates are used for copying the input data. Each Feynman gate produces two copies of input data bits. In the proposed design of the reversible ternary barrel shifter, the last stage of Modified Fredkin gate (MFG) does not require Feynman gates for copying data input bits or fan-outs. Thus in the (n, k) reversible ternary barrel shifter, if n is total number of input bits and k is the shift value then the number of ternary Feynman gates required to produce the desired fan-outs is *n(k-1)* as fan-out is needed in only k-1 stages. The MFG stages in a reversible ternary barrel shifter are responsible for shifting/rotating of data input bits. If k is the shift value for a (n,k) reversible ternary barrel shifter then it can be realized using minimum of k MFG stages. Each MFG stage has n number of Modified Fredkin gates (MFG) except for the last stage. The last stage of MFG requires only *n/2* number of

Modified Fredkin gates (MFG). Thus there are *k-1* stages which require n number MFG gates and the last stage requires *n/2* number of MFG Gates. Hence the total number of Modified Fredkin gates required to shift/rotate the input data is *n(k-1)+n/2* for a (n,k) barrel shifter.

A. Garbage Outputs

The MFG gate used in the reversible ternary barrel shifter at each stage produces at least one garbage output, except the last MFG gate which produces two extra garbage outputs. Thus for a (n,k) reversible ternary barrel shifter, the total number of garbage outputs (GO) is *GO=n(k-1)+(k+1).* Table I shows number of garbage output produced for different reversible ternary barrel shifter designs. In the table, n is the number of input data bits and k represents the shift value. It can be seen that there are 7 garbage outputs in (4:2) reversible ternary barrel shifter design that was illustrated in Fig. 7 are 7.

TABLE I. GARBAGE OUTPUTS FOR (N,K) REVERSIBLE TERNARY BARREL SHIFTER

n/k	n=4	n=8	n=16	n=32	n=64
k=2	7	11	19	35	67
k=3		20	36	68	132
k=4			53	101	197
k=5				134	262
k=6					327

B. Ancilla Bits

There are total of *n(k-1)* Feynman used in the design of (n,k) barrel shifter each having one ancilla bit. Further as can be seen from Fig. 7, 1 ancilla bit is needed for the MFG gates used in the design. Thus the total number of ancilla bits(AN) for proposed (n,k) reversible ternary barrel shifter design is *AN=n(k-1)+1.* For the design of a (4:2) reversible ternary barrel shifter shown in Fig. 7, there are 5 ancilla bits.Table II shows number of ancilla bits by varying the n and k values in (n,k) reversible ternary barrel shifter.

TABLE II. ANCILLA BITS FOR (N,K) REVERSIBLE TERNARY BARREL SHIFTER

n/k	n=4	n=8	n=16	n=32	n=64
k=2	5	9	17	33	65
k=3		17	33	65	129
k=4			49	97	193
k=5				129	257
k=6					321

C. Quantum Cost

As shown above, a reversible ternary barrel shifter can be realized using *n(k-1)+n/2* number of MFG gates and *n(k-1)* number of ternary Feynman gates, where n represents the number of bit and k represents the shift/control bit for a (n,k) reversible ternary barrel shifter. Thus the quantum cost (QC) of the (n,k) reversible ternary barrel shifter is: *QC=41*(n(k-1)+n/2)+4n(k-1).* Table III shows quantum cost calculated for different reversible ternary barrel shifter designs. The quantum cost of (4:2) reversible ternary barrel shifter shown in Fig. 7 is 268.

TABLE III. QUANTUM COST FOR (N,K) REVERSIBLE TERNARY BARREL SHIFTER

n/k	n=4	n=8	n=16	n=32	n=64
k=2	268	536	1072	2144	4288
k=3		904	1808	3616	7232
k=4			2544	5088	10176
k=5				6560	13120
k=6					16064

VI. CONCLUSIONS

In this paper, a novel architecture of a reversible ternary barrel shifter has been proposed. The proposed shifter is designed using ternary Feynman gates and Modified Fredkin Gates (MFG). The design of a reversible ternary barrel shifter is evaluated based on garbage output, ancilla bits and the quantum cost. For calculating quantum cost of the proposed design we have used the number of Muthukrishnan-Stroud gates and shift gates required in its implementation. The proposed reversible ternary barrel shifter will be of wide applications in reversible logic based digital signal processing systems.

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