

Design of a Comparator Tree Based on Reversible Logic

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Abstract—The existing design of reversible n-bit binary comparator that compares two n-bit numbers is a serial design [1] having the latency of $O(n)$. In this work, we present a new reversible n-bit binary comparator based on binary tree structure that has the latency of $O(\log_2(n))$. The reversible designs are based on a new reversible gate called the TR gate, the improved quantum cost of which is also derived in this work. In the proposed reversible binary tree comparator each node consists of a 2-bit reversible binary comparator that can compare two 2-bit numbers $x(x_i, x_{i-1})$ and $y(y_i, y_{i-1})$, to generate two 1-bit outputs Y and Z. Y will be 1 if $x(x_i, x_{i-1}) > y(y_i, y_{i-1})$, and Z will be 1 if $x(x_i, x_{i-1}) < y(y_i, y_{i-1})$. After careful analysis, we modified the logic equations of $Y = x_1\bar{y}_1 + kx_0\bar{y}_0$ and $Z = \bar{x}_1y_1 + k\bar{x}_0y_0$ to $Y = x_1\bar{y}_1 \oplus kx_0\bar{y}_0$ and $Z = \bar{x}_1y_1 \oplus k\bar{x}_0y_0$, respectively. The replacement of + operator with \oplus operator without affecting the functionality of the design helped us in reversible mapping of the equations of Y and Z on the third output of the TR gate which is $R = A\bar{B} \oplus C$. Further, TR gate can also efficiently generate functions such as $x_0\bar{y}_0$ and \bar{x}_0y_0 . In the proposed reversible binary comparator, the leaf nodes will consist of 2-bit reversible binary comparators. Each internal node (2-bit reversible binary comparator) of the binary tree receives the partial comparison results from the left and the right children and propagates the 2-bit output of the comparison to its parent. Finally, the root node which is also a 2-bit reversible binary comparator generates the 2-bit result of the comparison of the n-bit numbers x and y to evaluate whether $x > y$ or $x < y$. The 2-bit result of the root node are passed to the reversible output circuit designed from a Toffoli gate and 4 NOT gates to generate three signals $O_0(x < y)$, $O_1(x > y)$ and $O_2(x = y)$.

I. INTRODUCTION

Reversible circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between the input and output vectors. Reversible logic is considered as one of the promising practical strategies for power-efficient computing [2]. Reversible logic also finds application in emerging nanotechnologies such as quantum dot cellular automata, optical computing, etc [3], [4]. Another major applications of reversible logic lies in quantum computing as quantum networks must be built from reversible logical components [5], [6]. *Minimizing quantum cost, delay and the number of garbage outputs is the primary goal in reversible logic design and synthesis.* The garbage outputs are the unutilized outputs in reversible circuits which exist just to maintain reversibility but do not perform any useful operations.

The comparison of two binary number is one of the critical operations in many computing systems and finds wide

applications in general purpose microprocessors, communications systems, encryption devices, sorting networks etc [7]. Therefore, a reversible digital comparator should be carefully designed minimizing the quantum cost, delay and the number of garbage outputs. The design of quantum/reversible binary comparator has not been adequately referenced in the literature, and the design presented in [1] is the widely used design of the reversible binary comparator. In this work, we present a new design of the reversible binary comparator based on the binary tree structure having 2-bit reversible comparators as its nodes. The design is based on a new reversible gate called the TR gate, the improved quantum cost of which is also derived in this work. The TR gate is found to be very useful towards the design of binary comparator for minimizing the quantum cost, delay and the number of garbage outputs. The reversible design of 8-bit and 64-bit binary comparator based on the proposed approach is also illustrated. The proposed reversible tree based binary comparator is shown efficient in terms of quantum cost, delay and the number of garbage outputs compared to existing reversible binary comparator design proposed in [1].

The paper is organized as follows: Section II presents the basic reversible gates, quantum cost and their delay. Section III shows the existing design approach of designing the reversible binary comparator; Section IV presents the improved quantum cost and the delay of the reversible TR gate; Section V presents the design of the proposed reversible binary tree based comparator along with the design example for 8 bit and 64-bit comparators. Section VI concludes the paper.

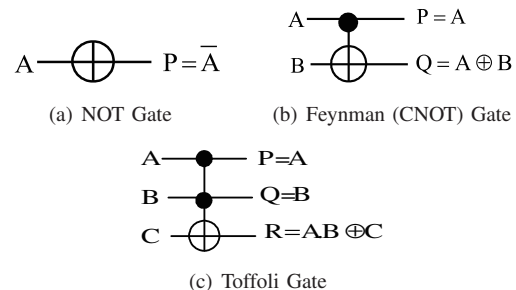


Fig. 1. Graphical representation of NOT, CNOT and the Toffoli gate

II. QUANTUM COST AND DELAY

The reversible gate has a cost associated with it called the quantum cost. The quantum cost of a reversible gate is the number of 1x1 and 2x2 reversible gates or quantum logic gates required in its design [5], [8]. The existing reversible gates used in this work are the NOT gate, the Feynman gate (CNOT gate) and the Toffoli gate which are shown in Fig. 1. The NOT and the Feynman gate have the quantum cost of 1 and the delay of 1Δ , while the Toffoli gate has the quantum cost of 5 and delay of 5Δ [9]. For delay calculations in the reversible logic circuits, the delay of all the paths to the outputs are first determined by summing up the delay values of the reversible gates in those paths. For example, if there are 5 paths to the outputs, the delay of the all these 5 paths are determined by summing up the delay values of the reversible gates in these 5 paths. Thereafter, the path to the output having the maximum delay value is chosen as the critical path and determines the propagation delay of the reversible circuit. The delay of the reversible gates and reversible circuits are discussed in detail in [9].

III. PRIOR WORK

The existing reversible design of the binary comparator is a serial architecture [1] that has the latency of $O(n)$. In the existing design approach, the comparator consists of a chain of reversible comparison cells that performs the operation of comparing a bit of the first number say x with the corresponding bit of the second number say y . In [1], a 1-bit comparator cell is designed using reversible Toffoli gates, Feynman gates and the NOT gates. The 1-bit reversible comparator cell is shown in Fig.2(a) while the output circuit is shown in Fig.2(b). The output circuit takes the two inputs $a_0(x < y)$ and $b_0(x > y)$ to generate three signals $O_0(x < y)$, $O_2(x > y)$ and $O_3(x = y)$. The reversible output circuit is designed from 1 Toffoli gate and 4 NOT gates. In the design presented in Fig.2(a), the reversible 1 bit comparator cell has 8 garbage outputs and has the quantum cost of 39 and delay of 24Δ (the delay is marked by dashed line in Fig. 2(a)). The reversible output circuit has the quantum cost of 9 and delay of 7Δ . The 8-bit and 64-bit reversible comparators can be designed by cascading 8 copies and 64 copies of the 1-bit comparator cell, respectively, followed by the reversible output circuitry. To illustrate an example of the existing reversible binary comparator, the design of the 3-bit comparator which compares two numbers x and y is shown in Fig.3 in which the x_2 and b_2 are the most significant bits. The outputs a_0 and b_0 are passed to the output circuit to generate three signals $O_0(x < y)$, $O_1(x > y)$ and $O_2(x = y)$. Using the serial design approach presented in [1], the 8-bit reversible comparator will have the quantum cost of 321, delay of 199Δ and generates 64 garbage outputs. The reversible design of the 64-bit reversible binary comparator will have the quantum cost of 2505, delay of 1543Δ and generates 512 garbage outputs.

IV. IMPROVED DESIGN OF TR GATE

The reversible TR gate is a 3 inputs 3 outputs gate having inputs to outputs mapping as $(P=A, Q=A \oplus B, R = A \cdot \bar{B} \oplus C)$

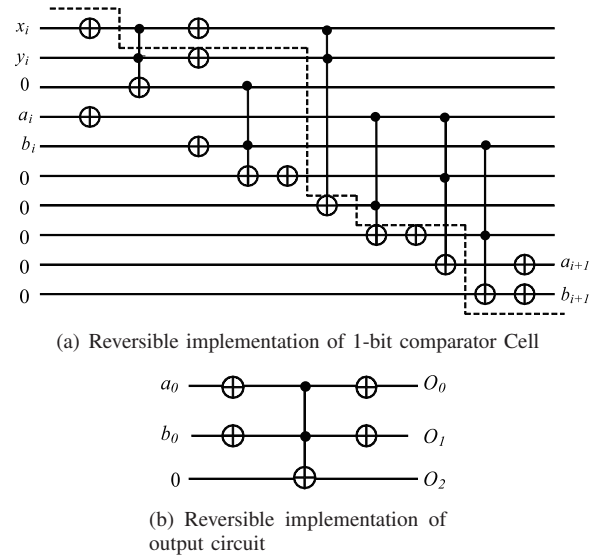


Fig. 2. Reversible designs of comparator cell and output circuit [1]

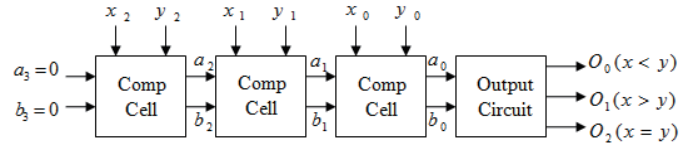


Fig. 3. Serial design of reversible 3-bit Comparator [1]

[10]. We present the graphical notation of the TR gate in Fig. 4(a) along with its new quantum implementation with 2x2 quantum gates in Fig. 4(b). The TR gate is designed from 1 Controlled V gate, 1 CNOT gate, and 2 Controlled V^+ gates resulting in its quantum cost as 4. Further, the logic depth of the quantum implementation of the TR gate is 4 resulting in its propagation delay as 4Δ . The quantum cost and the delay of the TR gate was earlier estimated as 6 and 6Δ , respectively [10]. The TR gate can realize the Boolean functions $A \cdot \bar{B} \oplus C$ and $A \oplus B$ with only gate. Further, it can implement the functions such as $A \cdot \bar{B}$ when its input C is tied to 0. These properties of TR gate make it very useful in designing the reversible binary comparator as illustrated in Section V.

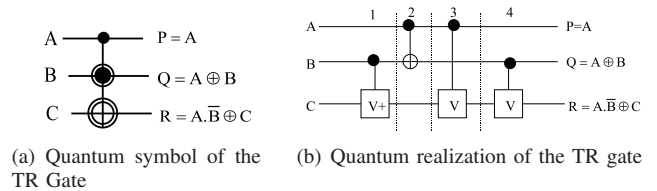


Fig. 4. TR gate and its improved quantum implementation

V. PROPOSED COMPARATOR DESIGN

We present a new reversible design of the binary comparator using the binary tree structure. The proposed design has the

latency of $O(\log_2(n))$. The proposed reversible binary tree comparator has a binary tree structure in which each node consists of a 2-bit reversible binary comparator that can compare two 2-bit numbers $x(x_i, x_{i-1})$ and $y(y_i, y_{i-1})$, to generate 2-bit outputs indicating whether $x(x_i, x_{i-1}) > y(y_i, y_{i-1})$ or $x(x_i, x_{i-1}) < y(y_i, y_{i-1})$. Thus, we propose a novel design of the 2-bit reversible comparator efficient in terms of quantum cost, delay and the number of garbage outputs. Each internal node (2-bit reversible binary comparator) of the binary tree receives the partial comparison results from the left and the right children and propagates the 2-bit outputs of comparison to its parent. Finally, the root node which is also a 2-bit reversible binary comparator generates the 2-bit comparison results of the two n-bit numbers x and y to evaluate whether $x > y$ or $x < y$. The 2-bit results of the root node is passed to the output circuit which was shown in Fig.2(b) to generate three signal $O_0(x < y)$, $O_1(x > y)$ and $O_2(x = y)$. The proposed approach is illustrated with the design of 8-bit and 64-bit reversible comparators.

A. Design of the 2-Bit Reversible Binary Comparator

For designing the 2-bit reversible binary comparator, consider two 2-bit binary numbers $x(x_1, x_0)$ and $y(y_1, y_0)$. The condition for $x > y$: $(x_1 > y_1)$ or $(x_1 = y_1 \text{ and } x_0 > y_0)$. Thus $Y = x_1\bar{y}_1 + kx_0\bar{y}_0$ should be 1 for $x > y$, where $k = x_1 \oplus y_1$ is 1 when $x_1 = y_1$. Similarly, the condition for $x < y$: $(x_1 < y_1)$ or $(x_1 = y_1 \text{ and } x_0 < y_0)$. Thus $Z = \bar{x}_1y_1 + k\bar{x}_0y_0$ should be 1 for $x < y$, where $k = x_1 \oplus y_1$ is 1 when $x_1 = y_1$. From the above equations of Y and Z we observed that to design the 2-bit reversible binary comparator we need to have the reversible module that can generate the outputs as $x_1\bar{y}_1$ and \bar{x}_1y_1 , the module is called R-Bcomp. Once we have R-Bcomp module ready it can also generate $x_0\bar{y}_0$ and \bar{x}_0y_0 by changing the inputs. We propose the reversible design of the R-Bcomp module using the reversible TR gate. TR gate is very useful as when its input C=0 we will have $R = A \cdot \bar{B}$ which can implement the logic functions such as $x_1\bar{y}_1$ and \bar{x}_1y_1 . Thus we used TR gate to design the R-Bcomp module as shown in Fig.5(a). In the R-Bcomp module the outputs \bar{x}_1y_1 and $x_1\bar{y}_1$ are labelled as a1 and b1, respectively. Further it can be observed that R-Bcomp also produces $\bar{k} = x_1 \oplus y_1$ which is beneficial in the design of 2-bit comparator.

After careful analysis, we modified the logic equations of $Y = x_1\bar{y}_1 + kx_0\bar{y}_0$ and $Z = \bar{x}_1y_1 + k\bar{x}_0y_0$ to $Y = x_1\bar{y}_1 \oplus kx_0\bar{y}_0$ and $Z = \bar{x}_1y_1 \oplus k\bar{x}_0y_0$, respectively. This is because since any function $F=A+BC$ will produce the same output as the function $F=A \oplus BC$ except when the variables A,B,C have the values as A=1,B=1 and C=1. In the equation of Y and Z explained above when k=1 then $x_1\bar{y}_1$ and \bar{x}_1y_1 will be 0 and vice versa, hence we are able to replace + operator with \oplus operator without affecting the functionality of the design. This helps in mapping of the equations of Y and Z on the third output of the TR gate which is $R=A\bar{B} \oplus C$. Since our R-Bcomp circuit shown in Fig. 5(a) produces the \bar{k} it can be passed as the B input of the TR gates to produce Y and Z signals without the need of the NOT gates. We use

the R-Bcomp shown in Fig.5(a) along with CNOT gate and TR gate to design the 2-bit reversible comparator as shown in Fig.5(b). The 2-bit reversible comparator has 6 garbage outputs(the unused outputs in the design) and has the quantum cost of 18 and delay of 18 Δ .

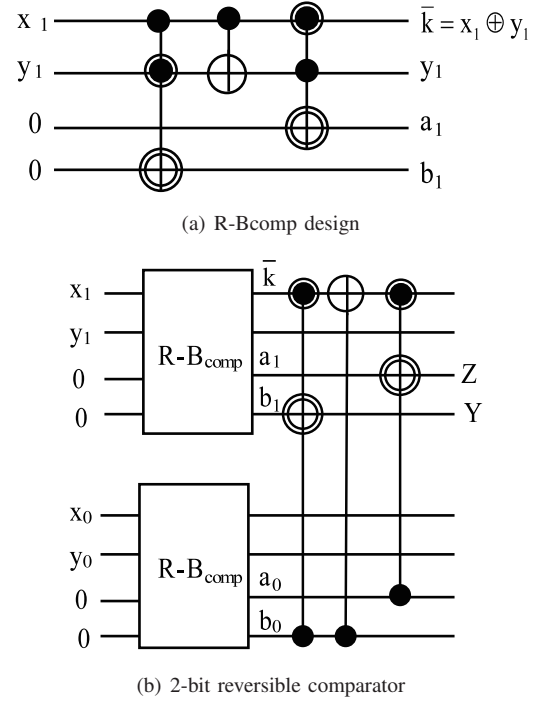


Fig. 5. Proposed design of 2-bit reversible comparator

B. Design of 8-Bit Reversible Binary Comparator

The proposed design of the 8-bit reversible comparator using reversible 2-bit comparator is shown in Fig.6 (the garbage outputs in the design are not shown). The design contains 2-bit reversible binary comparators as the nodes of the binary tree. Since $n=8$, the tree will have $\log_2(8)=3$ levels. The design requires seven 2-bit binary comparators along with a reversible output circuitry (R-O/P Ckt). The reversible output circuitry (R-O/P Ckt) is similar to the output circuit shown in Fig.2(b) and is primarily used to generate $O_2(x=y)$ signal from $x > y$ and $x < y$ outputs. The quantum cost of the proposed 8-bit reversible binary comparator is: $\{ 7 * \text{quantum cost of 2-bit binary reversible comparator} + \text{quantum cost of the reversible output circuitry} = 7 * 18 + 9 = 135 \}$. The delay of the 8-bit reversible binary comparators is: $\{ 3 * \text{delay of 2-bit binary reversible comparator} + \text{delay of the reversible output circuitry} = 3 * 18 \Delta + 7 \Delta = 61 \Delta \}$. The number of garbage outputs of the 8-bit reversible binary comparator is: $\{ 7 * \text{garbage outputs of the 2-bit binary reversible comparator} = 7 * 6 = 42 \}$. The improvement compared to the design presented in [1] for 8-bit comparator is shown in Table I.

C. Design of 64-Bit Reversible Binary Comparator

We also designed the 64-bit reversible comparator based on the binary tree based approach. The design will contain

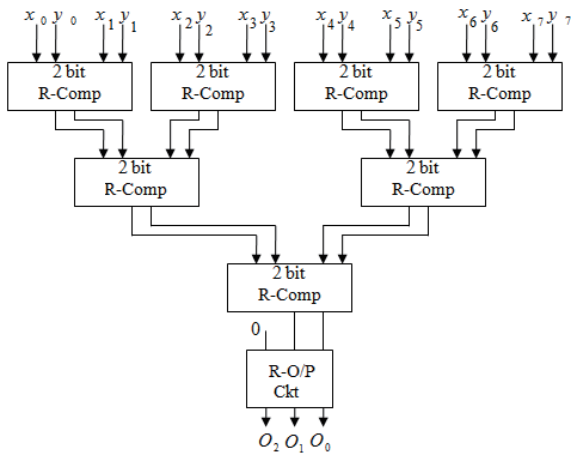


Fig. 6. Proposed reversible 8-bit comparator

TABLE I

A COMPARISON OF REVERSIBLE 8-BIT REVERSIBLE COMPARATOR

	QC	Delay	GOs
Serial Design [1]	321	199	64
Proposed Design	135	61	42
Improvement in %	57.94	69.34	34.37

nine 8-bit reversible binary comparator as illustrated in Fig.7 and the reversible output circuitry. The eight 8-bit reversible binary comparator are designed from 2-bit reversible binary comparators as illustrated in the Fig.6 with the difference that they will not contain the reversible output circuitries at the outputs. The proposed design of 64-bit reversible binary comparator will have the quantum cost of $\{ 9 * \text{quantum cost of 8-bit binary reversible comparator without the reversible output circuitry} + \text{quantum cost of the reversible output circuitry} = 9 * 126 + 9 = 1143 \}$. The delay of the 64-bit reversible binary comparators is: $\{ 2 * \text{delay of 8-bit binary reversible comparator without the reversible output circuitry} + \text{delay of the reversible output circuitry} = 2 * 54 \Delta + 7 \Delta = 115\Delta \}$. The number of garbage outputs of the 8 bit reversible binary comparator is: $\{ 9 * \text{garbage outputs of the 8 bit binary reversible comparator without the reversible output circuitry} = 9 * 42 = 378 \}$. Using the similar approach, the reversible n-bit tree based comparator can be designed. A comparison of the proposed reversible tree based comparator with the existing serial based approach [1] is illustrated in Table II for 64-bit binary comparator. We can see from Table II that the proposed design has an improvement of 92.7% compared to the design presented in [1] in terms of delay because of its logarithmic latency.

TABLE II

A COMPARISON OF REVERSIBLE 64-BIT COMPARATOR

	QC	Delay	GOs
Serial Design [1]	2505	1543	512
Proposed Design	1143	115	378
Improvement in %	54.37	92.5	26.17

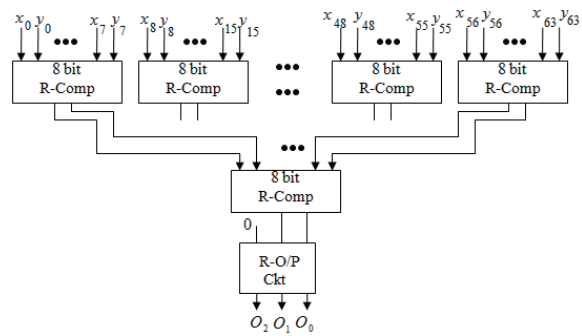


Fig. 7. Proposed reversible 64-bit comparator

VI. DISCUSSIONS AND CONCLUSIONS

We have presented reversible binary comparator based on binary tree based approach having logarithmic latency. The design is based on the useful properties of the TR gate suitable for mapping the comparator Boolean equations. The design presented is shown better than the existing serial design of reversible binary comparator in terms of quantum cost, garbage outputs and the propagation delay. Due to logarithmic latency, the proposed design achieves improvement of 92.7% in terms of delay compared to the existing serial design of 64-bit binary reversible comparator. The comparator designs proposed in this work can be useful in realizing the hardware design of the quantum algorithms such as Shor's factoring algorithm.

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