

Testable Reversible Latches for Molecular QCA

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Abstract— Nanotechnologies, including molecular QCA, are susceptible to high error rates. In this paper, we present the design of testable reversible latches (D latch, T Latch, JK Latch, RS Latch), based on reversible conservative logic for molecular QCA. Conservative reversible circuits are a specific type of reversible circuits in which there would be an equal number of 1s in the output as there would be on the input, in addition to one-to-one mapping. The proposed latches require only two test vectors, all 0s and all 1s, for detecting any unidirectional stuck-at faults. The design of QCA layouts and the verification of the latch designs performed using the QCA Designer tool are presented.

Keywords- Conservative reversible logic, molecular QCA, Latches

I. INTRODUCTION

Reversible circuits are those circuits that do not lose information, and reversible computation in a system can be performed only when the system consists of reversible gates. In reversible logic, there is one-to-one mapping between the input and output vectors and vice versa. Quantum dot cellular automata (QCA) is one of the possible technologies to implement the reversible logic. Due to significant error rates in nano-scale manufacturing, nanotechnologies including QCA require extremely low device error rate [1]. In literature, the testing properties of reversible logic are utilized on a one-dimensional array of molecular QCA [1]. In this work, we propose the design of testable reversible latches for molecular QCA using a special class of reversible logic called conservative reversible logic. In conservative reversible logic, in addition to one-to-one mapping, there would be an equal number of 1s in the output as there would be on the input. The advantage of reversible conservative logic is that it requires only two test vectors (all 0s and all 1s) to detect any unidirectional stuck-at faults in combinational circuits [2]. Moreover, the conservative logic is parity preserving, i.e., parity of the input is always equal to parity of the output [5]. The feedback in reversible sequential latches makes them untestable by all 0s and all 1s test vectors. Additionally, fan-out is not allowed in reversible logic. Hence, we propose a technique that will take care of the fan-out at the output of the reversible latches and can also disrupt the feedback to make them suitable for testing by only two test vectors, all 0s and all 1s. In other words, circuits will have feedback while executing in the normal mode. However, in order to detect faults in the test mode, our proposed technique will disrupt feedback to make conservative reversible latches testable as combinational circuits. Note that in existing literature, only the design of conventional irreversible RS latch exists for molecular QCA [5]. Thus, our work is significant because we are providing the

design for all types of latches completely testable for any unidirectional stuck-at faults by only two test vectors. Existing literature shows efforts to design reversible sequential circuits, but they are not based on conservative reversible logic [4]. Since the proposed conservative latches design requires only two test vectors to detect the faults, they will be of great importance in the nano-computing regime. The paper is organized as follows: Section II presents QCA defects and testing; Section III presents the conservative logic Fredkin Gate, basic QCA devices and also the QCA design of Fredkin conservative logic gate; Section IV shows the design of testable reversible latches; Section V describes the simulation conditions used to verify the designs along with simulation results; and Section VI provides the conclusions.

II. QCA DEFECTS AND TESTING

In the manufacturing of QCA, defects can occur in the synthesis and deposition phases. However, defects are more likely to take place during the deposition phase [8]. Researchers assume that QCA cells have no manufacturing defects, and that faults occur due to cell misplacement. These defects can be characterized as cell displacement, cell misalignment and cell omission [9]. Researchers have also considered missing/additional QCA cell defects [1]. In CMOS-based design, test sets based on the stuck-at model are used for finding faults, but they cannot completely detect the defects that happened during the fabrication process. The same is true for QCA. Single stuck-at fault test set cannot detect all QCA defects, due to the bridging faults between QCA cells. Hence, additional test vectors are required to cover the bridging faults [8, 9]. The two-vector testable conservative logic approach is based on the stuck-at fault model.

III. CONSERVATIVE REVERSIBLE FREDKIN GATE

All our designs are based on conservative reversible (3 input: 3 output) Fredkin Gate shown in Fig.1 [6]. Table 1 shows the truth table of Fredkin Gate and it can be seen that Fredkin gate produces the same number of 1s in the output as on the input, in addition to the one-to-one mapping feature of reversibility. Moreover, it is parity preserving [5]. Its input parity is equal to the output parity. Before showing the QCA design of Fredkin gate, we present the basic QCA logic devices: the majority voter (MV), the inverter (INV), binary wire and the inverter chain. Figures 2 and 3 show the basic QCA devices. The Launder four phase clocking scheme is generally used in QCA design, and our designs are also based on it. QCA design of Fredkin gate is shown in Fig. 4 using four-phase clocking scheme, in which the clocking zone is

shown by the number next to D (D0 means clock 0 zone, D1 means clock 1 zone and so on).

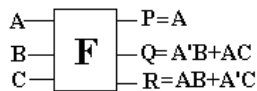


Figure 1. Fredkin Gate

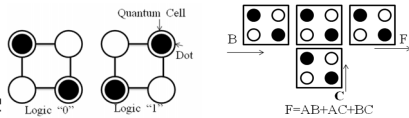


Figure 2. (a) QCA Cell (b) Majority Voter

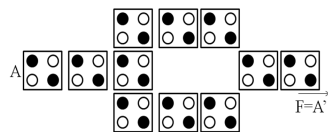
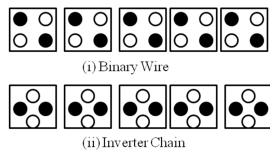


Figure 3. (a) Inverter



(b) Wires

TABLE I. TRUTH TABLE FREDKIN GATE

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

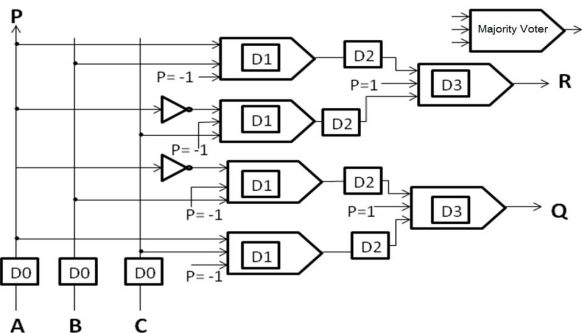


Figure 4. Fredkin Gate QCA design (D0 to D3 represent clock zones 0 to3)

IV. DESIGN OF TESTABLE REVERSIBLE LATCHES

The testable reversible latches are designed using the conservative reversible Fredkin gate.

A. D Latch

The characteristic equation of the D latch can be written as $Q^+ = D.E + E'Q$. The characteristic equation of the D latch can be mapped onto the Fredkin gate (F). Figure 5.a shows the realization of the reversible D latch using Fredkin gate. But fan-out is not allowed in reversible logic. Moreover, the design cannot be tested by two input vectors all 0s and all 1s because of feedback, as the output Q would latch 1 when the

inputs are toggled from all 1s to all 0s and could be misinterpreted as stuck-at-1 fault. We propose to cascade another Fredkin to output Q as shown in Fig. 5.b. The design has two control signals, C1 and C2. The design can work in two modes (a) normal mode (b) test mode. Normal Mode : In normal mode we will have C1C2=01 and we will have the design working as D latch without any fanout problem as shown in Fig.5.c. Test Mode (Disrupt the Feedback): In test mode , C1C2=00 will make it testable with all 0s input vectors as output T1 will become 0 and make it testable with all 0s input vectors. When C1C2=11 the output T1 will become 1 and the design will become testable with all 1s input vectors. It can be seen from above that C1 and C2 will disrupt the feedback in test mode, and in normal mode will take care of the fan-out. Thus our proposed design works as a reversible D latch and can be tested with only two test vectors, all 0s and all 1s, the inherent property of conservative reversible logic.

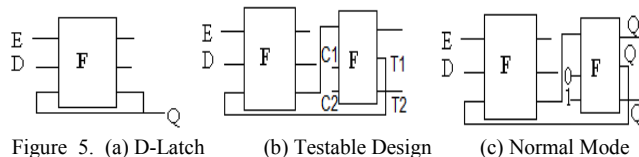


Figure 5. (a) D-Latch (b) Testable Design (c) Normal Mode

B. T Latch

The characteristic equation of the T latch can be written as $Q^+ = (T \oplus Q).E + E'Q$. But the same result can also be obtained from $Q^+ = (T.E) \oplus Q$. Figure 6.a shows the proposed design of reversible testable T latch with C1C2 as control signals as described in the section of D latch. The working of T latch in normal mode is shown in Fig.6.b having C1C2=01.

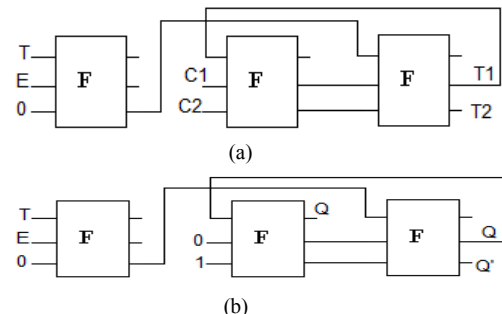


Figure 6. (a) Testable T Latch (b) Normal Mode

C. JK Latch

The characteristic equation of the JK latch can be written as $Q^+ = (JQ' + K'Q).E + E'Q$. After computing the equation $JQ' + K'Q$ it can be mapped on the D Latch to design the JK Latch. Figure 7.a shows the proposed design of testable JK latch with again C1C2 as the control signals. Its function in normal mode with C1C2=01 is shown in Fig.7.b

D. RS Latch

The characteristic equation of the RS latch can be written as $Q^+ = (S.E + (R.E)'Q)$. Figure 8.a shows the proposed design of the testable reversible RS latch with C1C2 as control signal. Here when C1C2=00 RS latch will work in test mode for all 0s input vectors. When C1C2=11, it will work in normal mode as well as test mode for all 1s input vectors as shown in Figure 8.b.

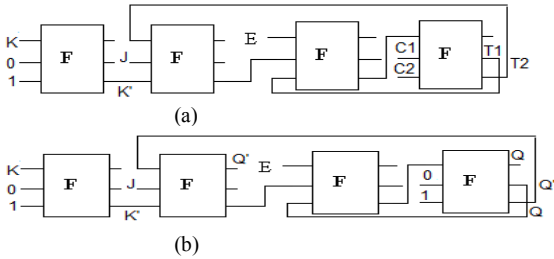


Figure 7. (a) Testable JK Latch (b) Normal Mode

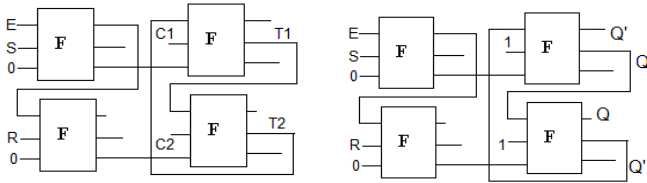


Figure 8. (a) Testable RS Latch (b) Normal Mode

V. SIMULATIONS

All the designs were verified using QCADesigner ver. 2.0.3 [7]. In the bistable approximation, we used the following parameters: cell size=18 nm, number of samples=42800, convergence tolerance =0.001000, radius of effect=41 nm, relative permittivity=12.9, clock high=9.8e-22, clock low=3.8e-23, clock amplitude factor=2.000, layer separation=11.5000nm, maximum iterations per sample=200. In our QCA layouts, we have the goal of workable designs with compact layouts. Each Fredkin gate in the layouts will delay the output by one cycle (Fredkin Gates in the critical path). Figures 9 and 10 show the QCA layout of Fredkin gate and simulation results, respectively, drawn on QCADesigner tool (We have not shown the output P as it is a simply a wire connection). Figures 11 and 12 show the QCA layout and simulation results of D latch, respectively. In Figures 11 and 12, O1 and O2 represent the intermediate output; we have used the intermediate output so that the readers can better understand the simulation results and the work can be reproduced by others (the actual outputs are named as Q and QBAR). Figures 13 and 14 show the QCA layout and simulation results of T latch, respectively. In Figure 13, we have used QBAR (complement of output Q) for feedback rather than Q to make the layout compact. Again, intermediate output is also shown in the layout and simulation for better understanding. Figures 15 and 16 show the QCA layout and simulation results of JK latch, respectively. Figure 17 shows the QCA layout of RS latch.

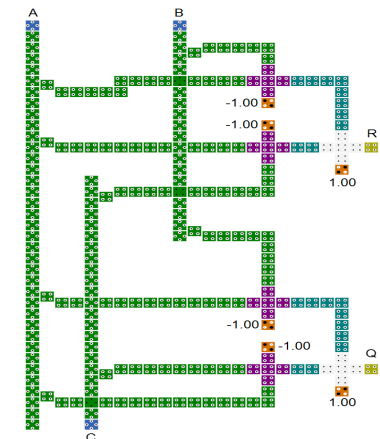


Figure 9. QCA Layout of Fredkin Gate

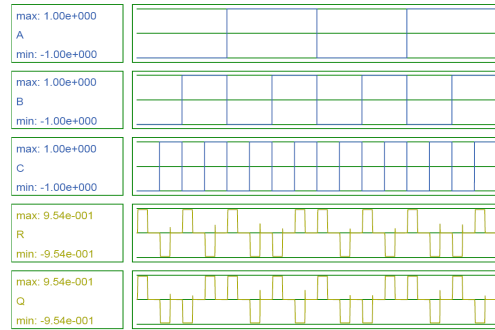


Figure 10. Simulation of Fredkin Gate

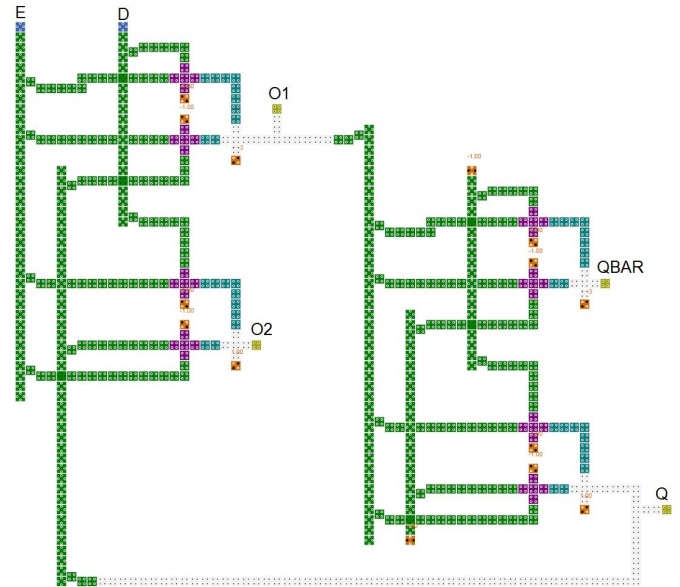


Figure 11. QCA Layout of D Latch

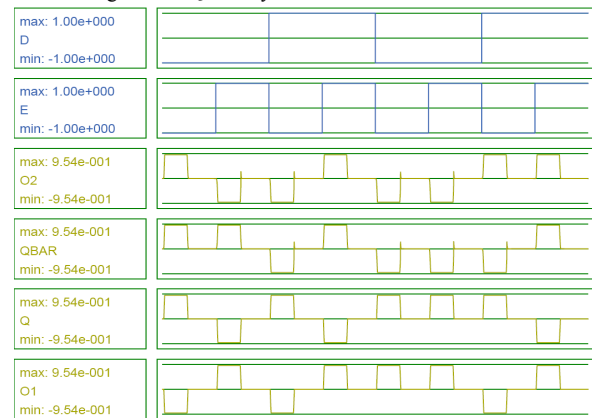


Figure 12. Simulation of D Latch

VI. CONCLUSIONS

We propose the design of testable conservative reversible latches (D Latch, T Latch, JK Latch and RS Latch) for molecular QCA. Conservative logic is testable for any unidirectional stuck-at faults using only two test vectors, all 0s and all 1s. The proposed conservative reversible latches have feedback that deters their testing by only two test vectors, thus

a technique is demonstrated to disrupt the feedback in test mode. In conclusion, the proposed conservative latch designs require only two test vectors to detect any unidirectional stuck-at faults, and will be of great importance to nano-computing.

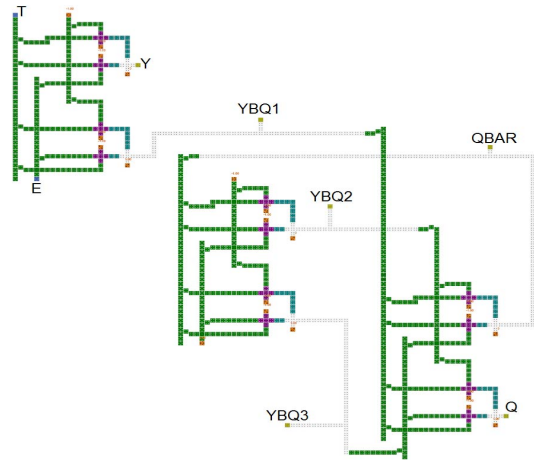


Figure 13. QCA Layout of T Latch

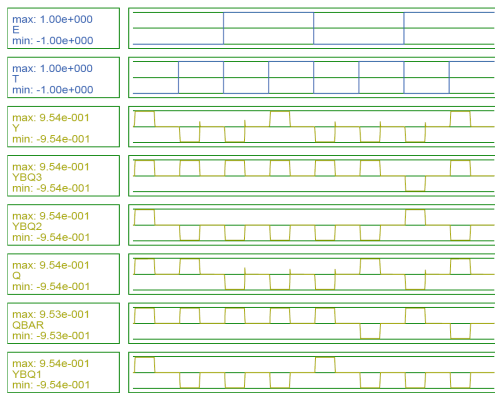


Figure 14. Simulation of T Latch

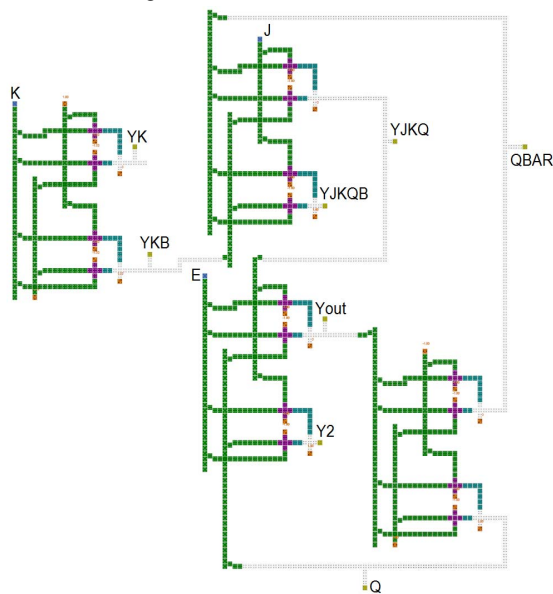


Figure 15. QCA Layout of JK Latch

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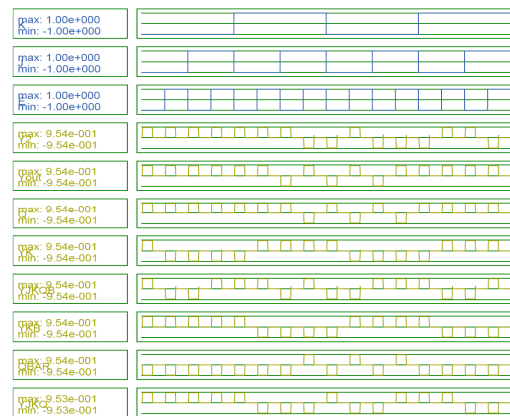


Figure 16. Simulation of JK Latch

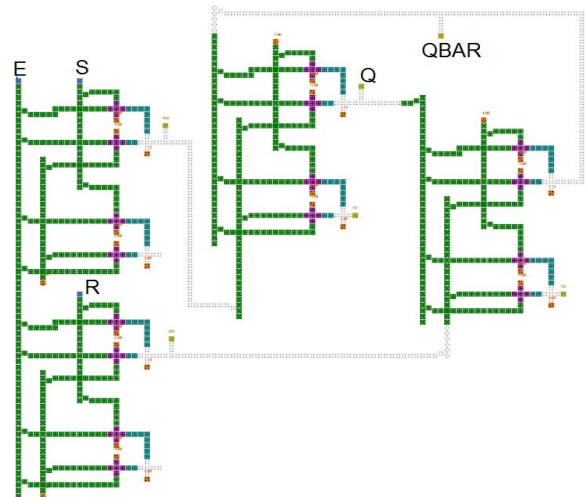


Figure 17. QCA Layout of RS Latch