

Concurrently Testable FPGA Design for Molecular QCA Using Conservative Reversible Logic Gate

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Abstract—Reversible logic is attracting the researchers attention for fault susceptible nanotechnologies including molecular QCA. In this paper, we propose concurrently testable FPGA design for molecular QCA using conservative reversible Fredkin gate. Fredkin gate is conservative reversible in nature, in which there would be an equal number of 1s in the outputs as there would be on the inputs, in addition to one-to-one mapping. Fault patterns in Fredkin gate are analyzed using HDLQ tool due to a single missing/additional cell defect in molecular QCA. Exhaustive simulation shows that if there is a fault in molecular QCA implementation of Fredkin gate, there is a parity mismatch between the inputs and the outputs; otherwise the inputs parity is same as outputs parity. Thus, any permanent and transient fault in molecular QCA that results in parity mismatch can be concurrently detected. The logic block and the routing fabric (both are programmable) are the two key components of an FPGA. Thus, we have shown the Fredkin gate based concurrently testable designs of the configurable logic block (CLB) and the routing switch of a molecular QCA-based FPGA. Analysis of power dissipation in the proposed FPGA is also shown.

I. INTRODUCTION

Quantum dot cellular automata (QCA) is one of the emerging nanotechnologies that has extremely small feature size, higher clock frequency and consumes ultra low power [1]. QCA provides an alternative way of computation in which the logic states ('0' and '1') are defined by the position of electrons. Due to significant error rates in nano-scale manufacturing, nanotechnologies including QCA require extremely low device error rate [2]. In the manufacturing of QCA, defects can occur in the synthesis and deposition phases. However, defects are more likely to take place during the deposition phase [3]. QCA devices are also prone to transient faults as the energy difference between the ground and the excited state is small [4]. Field programmable gate arrays (FPGAs) have emerged as a promising technology in key areas such as the development of high-performance embedded systems, DSP, software-defined radio and bioinformatics. FPGA design using QCA has attracted the attention of researchers due to its computationally useful and general-purpose nature. The existing works on QCA-based FPGA are concentrated either on programmable interconnects or on programmable logic [5], [6]. To the best of our knowledge, the concurrent testing of faults in QCA-based FPGA has not been addressed in the literature. *Concurrent testability is defined as the property of circuits in which faults can be detected at run time while the circuit is performing the normal operations.* In this work, we are proposing concurrently testable FPGA design for molecular QCA using conservative reversible logic gate (Fredkin gate). In conservative reversible logic, there would be equal number of 1s in the outputs as there would be on the inputs, in addition to one-to-one mapping between input and output vectors [7]. Conservative reversible logic is different from conservative logic as conservative logic may be reversible or may not be reversible in nature, but conservative reversible logic will always be reversible [8]. Reversible circuits do not lose information. Reversible circuits are dissipation less circuits working even beyond the thermodynamic

limit of $kT \ln 2$ energy dissipation, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [9], [10].

In literature, the testing properties of reversible logic are utilized on a one-dimensional array of molecular QCA [2]. In this work, we have investigated reversible logic for concurrent testing of fault in QCA-based FPGA. We performed the fault pattern study of reversible Fredkin gate due to a single missing cell defect and the additional cell defect in QCA. We found that when there is a permanent fault due to above defects, there is a parity mismatch between the inputs and the outputs of the Fredkin gate, i.e., the parity of the inputs will not be same as the parity of the outputs. Due to parity preserving property, any permanent and transient fault in molecular QCA that results in parity mismatch can be concurrently detected. The logic block and the routing fabric (both are programmable) are the two key components of an FPGA. Hence, the Fredkin gate based concurrently testable configurable logic block (CLB) and the routing switch of a QCA-based FPGA design are designed. The CLB of an FPGA internally consists of basic logic elements (BLEs) designed from lookup tables (LUTs), memory elements and D flip-flops. Thus concurrently testable design of LUT, memory element and D flip-flop are also presented for molecular QCA-based FPGA. QCA layouts and the verification of the proposed work using the QCADesigner [11] and HDLQ [12] tools are presented. Analysis of power dissipation in the proposed FPGA is also performed by synthesizing MCNC benchmark functions in the FPGA CAD tools.

The paper is organized as follows: Section 2 presents conservative reversible Fredkin gate; Section 3 presents proposed concurrent testing methodology; Section 4 discusses concurrently testable CLB design; Section 5 presents concurrently testable routing switch of a QCA-based FPGA; Section 6 discusses simulations and verification of the proposed designs and the power analysis of the proposed FPGA; Section 7 provides the conclusions.

II. CONSERVATIVE REVERSIBLE FREDKIN GATE

The designs presented in this work are based on the conservative reversible (3 inputs: 3 outputs) Fredkin Gate shown in Fig. 1 [7]. Fredkin gate can be described as mapping (A, B, C) to $(P=A, Q=A'B+AC, R=AB+A'C)$, where A, B, C are inputs and P, Q, R are outputs, respectively. It can be seen that Fredkin gate produces the same number of 1s in the outputs as on the inputs, in addition to the one-to-one mapping feature of reversibility. Moreover, it is parity preserving. Its inputs parity is equal to the outputs parity. The QCA technology is based on QCA logic devices: the majority voter (MV), the inverter (INV), binary wire and the inverter chain. Figure 2 shows the basic QCA devices. The proposed designs are based on the Landauer four phase clocking scheme, as common in most QCA designs. A simple and elegant tutorial on QCA can be found in [11]. Due to limitation of space we are only showing the QCA design of

the Fredkin gate in Fig. 3 using 4 phase clocking scheme(D0,D1,D2 and D3 are the 4 clocking zones and MV represents the majority voter). Please refer Fig.9 of our paper in [13] for Fredkin gate QCA layout.

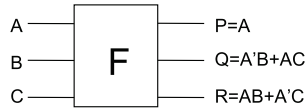


Fig. 1. Fredkin Gate

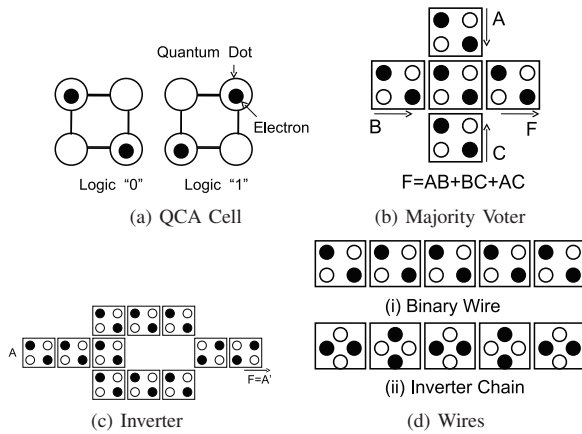


Fig. 2. QCA Cell and Basic QCA Devices

III. PROPOSED CONCURRENT TESTING METHODOLOGY

Researchers have proved that molecular QCA cells are more susceptible to missing/additional QCA cell defects. In this work, our analysis is also based on single missing/additional QCA cell defect [3]. The exhaustive testing of the Fredkin gate QCA layout shown in our paper in [13](please refer Fig. 9 in [13], is done with the presence of all possible single missing/additional cell defects in MV, INV, fan-out, Crosswire and L-shape wire [12]. This generated 20 unique fault patterns at the outputs as shown in Table I. In Table 1, ai is the 3 bit pattern having an equivalent decimal value of i, thus a0 represents 000 (decimal 0), a1 represents 001(decimal 1),..., a7 represents 111(decimal 7). The fault pattern study is done

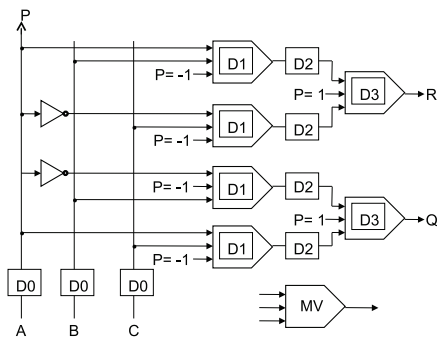


Fig. 3. QCA Layout of Fredkin Gate

by modeling QCA layout using HDLQ [12], a design tool which provides the Verilog HDL library of QCA devices, i.e., MV, INV, fan-out, Crosswire, L shape wire with fault injection capability. We carefully observed each fault pattern and found that in the occurrence of a fault, there is a parity mismatch between the outputs and the inputs of the Fredkin gate (i.e., parity of the input vector is not equal to the output vector). This led us to conclude that Fredkin gate can concurrently detect a permanent fault by matching the parity. Since Fredkin gate is logically parity preserving, it can also detect the transient faults which result in parity mismatch. Hence, Fredkin gate can concurrently detect a permanent, as well as, a transient fault in molecular QCA based on parity preserving property.

IV. CONCURRENTLY TESTABLE CONFIGURABLE LOGIC BLOCK (CLB) DESIGN

The logic block and the routing fabric (both are programmable) are the two key components of an FPGA. The logical functions are implemented using logic blocks (configurable logic blocks) whereas the interconnections are made through the routing fabric. The configurable logic block (CLB) internally consists of basic logic element which in turn is designed from lookup table; memory element and a D flip-flop.

A. Design of Fredkin gate Based Lookup Table (LUT)

An n input lookup table can realize any n input Boolean function and is designed by a m:1 multiplexer (where $m = 2^n$) and m 1-bit storage cells. It is a well-known fact that m:1 multiplexer can be implemented with m-1 2:1 multiplexers. Fredkin gate has two of its outputs as 2:1 multiplexers, thus multiplexer based approach of designing the LUT is very much suited for designing concurrently testable LUT for molecular QCA. An example of 3 inputs LUT using Fredkin gate as a 2:1 multiplexer is shown in Fig. 4. It requires 7 reversible Fredkin gates and 8 1-bit memory cells to design 3 inputs look up table. The design of a memory cell will be discussed in the next sub-section.

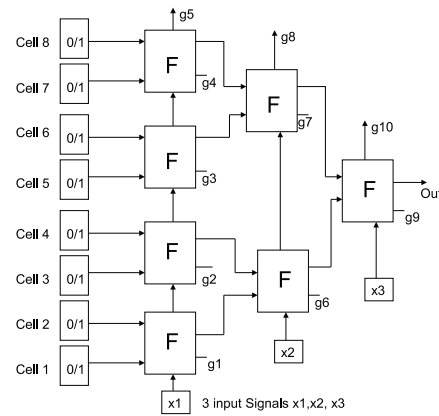


Fig. 4. 3 Inputs Concurrently Testable Lookup Table Designed using 7 Fredkin Gates(F) and 8 1-bit Reversible Memory Cells

B. Design of Concurrently Testable 1-bit Memory Cell

We have used D-Latch as a memory cell in the QCA-based FPGA, as Fredkin gate can be easily modelled as a D-Latch. The characteristic equation of the D latch can be written as $Q^+ = D \cdot E + \bar{E} \cdot Q$ [13]. It can be mapped onto the Fredkin gate (F). Figure 5(a) shows the realization of the reversible D latch using

TABLE I
FAULT PATTERNS IN FREDKIN GATE

Input Vector	Fault Free	Fault Patterns																			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
a0	a0	a0	a0	a1	a1	a0	a0	a1	a2	a1	a1	a0	a2	a0	a2	a0	a0	a0	a2	a4	
a1	a1	a1	a1	a1	a1	a0	a1	a0	a1	a1	a1	a1	a3	a1	a3	a3	a3	a3	a3	a5	
a2	a2	a3	a2	a2	a3	a2	a0	a3	a2	a3	a3	a2	a0	a0	a2	a2	a2	a2	a0	a6	
a3	a3	a3	a3	a3	a3	a2	a1	a2	a1	a3	a3	a3	a1	a1	a3	a3	a3	a3	a1	a7	
a4	a4	a4	a5	a5	a5	a4	a4	a4	a4	a5	a4	a4	a4	a4	a4	a6	a4	a6	a4	a0	
a5	a6	a6	a7	a7	a7	a7	a6	a6	a6	a6	a6	a6	a6	a6	a6	a4	a4	a4	a6	a2	
a6	a5	a4	a4	a5	a4	a5	a5	a5	a5	a5	a5	a4	a5	a7	a5	a5	a5	a7	a5	a1	
a7	a7	a6	a6	a7	a6	a7	a7	a7	a7	a7	a7	a6	a7	a7	a7	a5	a5	a7	a7	a3	

Fredkin gate (fan-out is not allowed in reversible logic but fanout is allowed in molecular QCA). It requires only 1 Fredkin gate to implement D-Latch in QCA.

C. Design of Testable D Flip-flop

D flip-flop is another integral component of the basic logic element of concurrently testable QCA-based FPGA. Figure 5(b) shows the design of conservative reversible master-slave flip-flop in which the testable D latch shown in Fig. 5(a) is cascaded in master-slave fashion for its design. Master-slave D flip-flop is designed with 3 Fredkin gates as fan-out is allowed in QCA design. While designing the QCA layout of sequential circuits we have made sure that the signals arrive at the same time to the Fredkin gates input. This is done by inserting the delays.

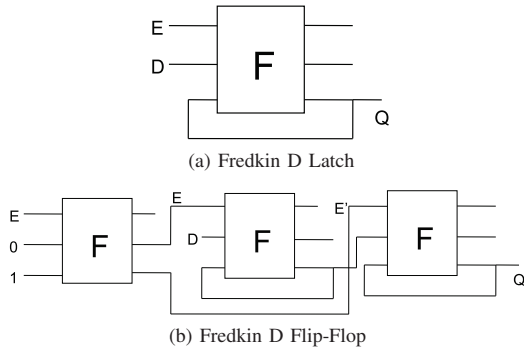


Fig. 5. Fredkin Sequential Circuits

D. Design of Testable FPGA Basic Logic Element(BLE)

One BLE consists of a LUT (lookup table), a D-FF and a 2:1 MUX. The Fredkin gate based 3 inputs LUT, Fredkin gate based D flip-flop, and a Fredkin gate working as a 2:1 MUX are combined to design the basic logic element of concurrently testable QCA-based FPGA. The design is shown in Fig. 6.

E. Design of Concurrently Testable Configurable Logic Block (CLB)

The configurable logic block (CLB) of the proposed FPGA is designed by clustering the basic logic elements. In the existing literature, the cluster based CLB architecture is well implemented in conventional technologies like CMOS [14]. We are also using the cluster-based approach of designing the CLB from basic logic elements (BLEs). An illustration of the concurrently testable CLB design for molecular QCA is shown in Fig. 7. In Fig.7, one CLB includes 3 BLEs (basic logic elements) and 5 inputs and 3 outputs. In Fig. 7, FLUT represents 3 inputs lookup table based on Fredkin gate;

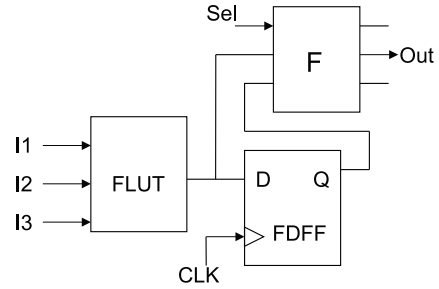


Fig. 6. Proposed Design of LUT-Based Logic Element for QCA-Based FPGA

F-DFF is a Fredkin gate based D flip-flop; F2:1 and F8:1 represents 2:1 and 8:1 multiplexers, respectively, designed from Fredkin gate; FAND is a AND gate designed from Fredkin gate; FNOT is an inverter designed from Fredkin gate and Mcell is the memory cell designed from Fredkin gate.

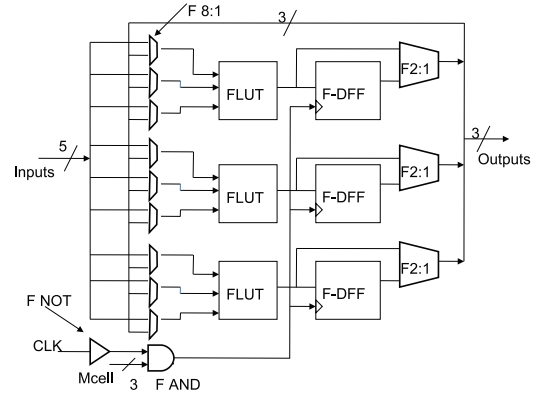


Fig. 7. Proposed Concurrently Testable CLB Design using Clustering Approach

F. Concurrently Testable Rotating Switch for QCA-Based FPGA

The FPGA routing switch consists of a n:1 multiplexer, a buffer and SRAM configuration cells, as shown in Fig. 8(a). The inputs to the multiplexer comes from the other routing conductors in the network or from the logic block outputs. The output of the buffer can be connected to a routing conductor or to a logic block input. In the routing switch, the programmability to select the input signal is realized through the SRAM configuration cells. As discussed above n:1 multiplexer can be implemented with n-1 2:1 multiplexer

thus requiring $n-1$ Fredkin gates. The required SRAM cells can be configured as 1-bit memory cells designed as D latches from Fredkin gate. The buffer is required in conventional FPGAs to restore the signals as the switches are implemented with pass transistor logic. We don't require any buffer in QCA implementation. A demonstration of the proposed approach of designing concurrently testable routing switch is shown in Fig.8(b) for 4 inputs.

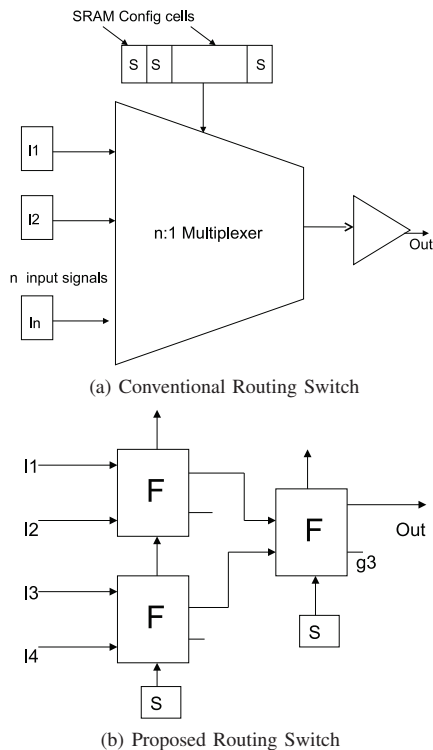


Fig. 8. Design of Routing Switch

V. SIMULATIONS FOR VERIFICATION

QCADesigner ver. 2.0.3 [11] and HDLQ [12] are used for simulation and verifying the designs. QCADesigner is used to design and accurately simulate small and key building blocks like Fredkin gate, Fredkin testable block, D latch and D flip-flop. To validate the proposed approach of designing the LUT and the routing switching, 2 input LUT and 4 input routing switch is also simulated in QCA designer tool. (2 input LUT is simulated for evaluation in QCA designer because of its less complexity). In the bistable approximation using QCA designer tool, we used the parameters mentioned in [13]. In this work, HDLQ is used for designing and simulating larger and complex systems such as complete design of 3 inputs LUTs with memory elements. HDLQ is chosen to verify and simulate complex designs as Verilog HDL library of QCA gates are available and thus complex designs can be simulated for verification by coding in Verilog HDL.

An important objective in our work is to approximate the power dissipation in the proposed QCA-based FPGA as there is no QCA tool available for power analysis. Recently in [15], an upper bound is provided for the power dissipation in QCA circuits. In [15], it is shown that over different inputs combinations, the maximum power dissipation in QCA majority gate is approximately 71.99

meV. We synthesized MCNC benchmark functions in the proposed FPGA having 4 inputs LUT(4-LUT) based BLEs using CAD flow mentioned in [14]. This gives us the number of BLEs required by each benchmark function. Each 4 inputs BLE will require 35 Fredkin gates (31 Fredkin gates for 4-LUT, 1 Fredkin gate as a 2:1 Mux and 3 Fredkin gates for D flip-flop). Each Fredkin gate requires 6 majority QCA gates, thus 4 inputs BLE will have maximum power dissipation of $35 \times 71.99 \times 6 \text{ meV} = 15.117 \text{ eV}$. We computed the power dissipation of various synthesized MCNC benchmarks by multiplying the number of BLEs required by each with the power dissipation in each BLE. It is observed that the maximum power dissipation is for clma benchmark function having value of $125.742 \times 10^3 \text{ eV}$. Hence, the power dissipation in proposed QCA-based FPGA is in eV that is negligible compared to a conventional CMOS FPGA.

VI. CONCLUSIONS

Concurrently testable FPGA design for molecular QCA is presented based on conservative reversible Fredkin gate. The complete concurrently testable designs of the configurable logic block and the routing switch of the QCA-based FPGA are shown. All the designs are functionally verified using the QCA simulation tools. The proposed work is the starting point for designing concurrently testable reconfigurable systems in molecular QCA computing.

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