BIT CONSERVING LOGIC AS A POTENTIAL INTEGRATION PLATFORM FOR HYBRID MOLECULAR & NANOSCALE CMOS-BASED ARCHITECTURES

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ABSTRACT: The existing CMOS technology is reaching its limits beyond which the down scaling in feature size and proper working of the device is becoming extremely difficult. Nanotechnologies such as quantum computing, carbon nanotubes-based field effect transistors (CNTFET) and quantum dot cellular automata (molecular and magnetic) are being explored as the potential alternative to CMOS. It looks very unlikely in the current scenario that CMOS will completely be taken over by these emerging technologies because of research advancement and economic impact of CMOS based devices. Hence, the integration of CMOS with these emerging nanotechnologies in complementary manner seems one of the viable alternatives to continue the Moore's law. One of the challenges in integration lie in the fact that each emerging technology has a different fault model thus logic designers should come with a common platform in which the same design methodology and tools can be used for design. The common platform should work for the different fault models without changing the design methodology and should perform well on metrics such as power, speed, area and fault testing. In this work, we propose the use of bit conserving logic as a platform to integrate CMOS with the emerging technologies such as carbon nanotubes-based field effect transistors (CNTFET) and quantum dot cellular automata because of potential advantages of bit conserving logic circuits for concurrent testing (online testing) of faults irrespective of technology in which it is implemented.

In bit conservative logic, there would be an equal number of 1s in the outputs as there would be on the inputs. Thus, bit conservative logic circuits are parity preserving, that is, the parity of the input vectors is equal to that of the output vectors [1]. Thus if there is a *single permanent or transient fault* in the implementation of bit conservative logic circuit that results in parity mismatch between the inputs and the outputs, it can be concurrently detected by comparing the parity of the input and the output vectors. Thus bit conservative logic can provide a novel design platform for integration of CMOS with emerging technologies in which parity preserving property will be the concurrent fault detection scheme. In this work, we will propose novel gates or computing element based on bit conserving logic for different technologies such as CMOS, quantum dot cellular automata (QCA) and carbon nanotubes-based field effect transistors. In the preliminary study, we have performed the study on bit conservative logic for concurrent fault detection in *molecular QCA computing and proved that bit conservative computing implemented in molecular QCA results in concurrent detection of single missing/additional cell defects in molecular QCA [2, 3]*. In the present work, our focus will be on designing bit conservative logic gates in CMOS and CNTFET, and to demonstrate how bit conservative logic can provide a platform for integration of hybrid molecular and CMOS based design. Bit conservative logic can also be reversible in nature if the bit conservative logic gate also satisfies the reversible property of one-to-one mapping between the input and output vectors. One of the most popular reversible logic gates called Fredkin gate is also bit conservative in nature. *This makes the proposed work also beneficial for emerging nanotechnologies such as quantum computing which are reversible in nature and the low power concurrently testable VLSI design based on bit conservative reversible logic*.

REFERENCES:

[1] G. Swaminathan, J. Aylor, B. Johnson, "Concurrent Testing of VLSI circuits using Conservative logic,", Proc. International Conference on Computer Design (ICCD), 1990, Cambridge, MA, Sep 1990, pp 60-65.

[2] H. Thapliyal and N. Ranganathan, "Reversible Logic Based Concurrently Testable Latches for Molecular QCA", To appear IEEE Trans. on Nanotechnology, 2009.

[3] H. Thapliyal and N. Ranganathan, " Conservative QCA Gate (CQCA) for Designing Concurrently Testable Molecular QCA Circuits", Proc. of the 22nd International Conference on VLSI Design , Delhi, India, Jan 2009,pp.511-516.